A Flash-ADC data acquisition system developed for a drift chamber array and a digital filter algorithm for signal processing*

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Abstract: A Flash-ADC data acquisition (DAQ) system has been developed for the drift chamber array designed for the External-Target-Experiment at the Cooling Storage Ring at the Heavy Ion Research Facility, Lanzhou. The simplified readout electronics system has been developed using the Flash-ADC modules and the whole waveform in the sampling window is obtained, with which the time and energy information can be deduced with an offline processing. A digital filter algorithm has been developed to discriminate the noise and the useful signal. With the digital filtering process, the signal to noise ratio (SNR) is increased and a better time and energy resolution can be obtained.

Keywords: external target experiment, multiwire drift chamber, flash-ADC, DAQ

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1 Introduction

The Cooling-Storage-Ring (CSR) [1] has been built at the Heavy Ion Research Facility, Lanzhou (HIRFL). The heavy ion beams with energy below 1 GeV/u offer opportunities to study the properties of nuclear matter and radioactive beam physics [2–5]. The beam accelerated by the main ring of CSR is guided to the External-Target-Experiment terminal through the Radioactive Ion Beam Line Lanzhou-II (RIBLL-II) [6]. At the experiment terminal a large universal spectrometer detector system is designed to study the properties of nuclear matter at low temperature and high baryon density [3]. Fig. 1 displays the conceptual design of the CSR External-Target-Experiment (CEE). The drift chamber array is the key tracking detector to reconstruct the momentum of the particles emitted at forward rapidity produced in the collisions between incident beam and fixed target.

The array consists of two arms located downstream of the dipole magnet. Each arm consists of three drift chambers, as shown in Fig. 1 [7]. The angles between the incident beam and the normal direction of each arm are -15° and $+15^\circ$ respectively. The drift chamber array covers the main solid angle region that is important for the physics purpose.

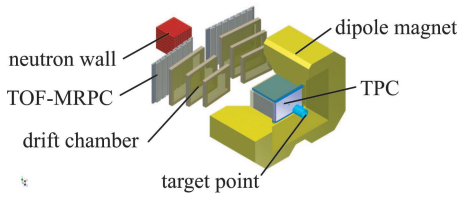

Fig. 1. The layout of the External-Target-Experiment spectrometer system.

Before the final manufacture of the drift chamber array, a prototype should be built and tested with beam to make sure that the structure design satisfies the requirements both in spatial resolution and energy resolution. First, a small prototype with sensitive area of 80 mm × 80 mm was designed and tested [7]. After showing that the performance of the small prototype satisfies the design requirements, a large prototype with sensitive area of 325 cm × 420 cm was designed for test and presented in this paper. The large prototype was first tested using cosmic-rays and then tested with a pion and proton beam

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at the E3-Line at Institute of High Energy Physics [8]. The beam momenta used in the test were 400 MeV and 500 MeV, and the particle event rate is about 100/min. For the test of the prototype array, the Flash-ADC DAQ was designed and the performance of the system was tested. Compared with a traditional DAQ system based on NIM and CAMAC electronics, the Flash-ADC DAQ system has a smaller electronics volume and is more flexible in event analysis with complex waveforms. A set of digital filter algorithm is developed for the signal processing to increase the Signal-Noise-Ratio. The structure of the drift chamber is described in Section 2. In Section 3 the DAQ system and the test results are introduced. The digital signal processing is introduced in Section 4 and some primary results are introduced in Section 5.

2 Structure of the drift chamber

Each prototype drift chamber consists of three sense wire planes. The wires in the first plane are stretched in the perpendicular direction and the wires in the other two planes are rotated by $+30°$ and $-30°$ relative to the wires in the first plane respectively. Each sense wire is surrounded by field wires which form a drift cell, as shown in Fig. 2.

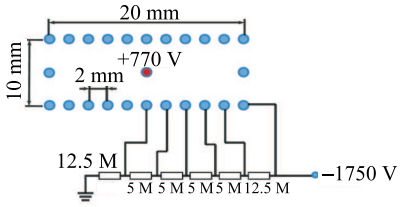

Fig. 2. The structure of a drift cell.

A positive voltage of +770 V is added to the sense wire and the field voltage is set as −1750 V at the edge wires and increases gradually towards to the center through the voltage bleeder.

The material of the sense wire is gold-plated tungsten with a diameter of 20 μm and Be-plated wire is selected as the field wire [9]. The working gas of the chamber is a mixture of argon and carbon dioxide (85:15). The gas flow is controlled at about 150 mL/min, which can prevent the contamination of oxygen or water vapor in the chamber gas component.

3 Readout electronics and DAQ system

3.1 Drift chamber preamplifier

For high precision drift time measurement, a voltage-sensitive preamplifier with common-base transistor input is designed for the drift chamber. The preamplifier has a high voltage gain of the order of 10^2 and a high bandwidth that is suitable for amplifying fast signals produced by the chamber. The signal has a rise time of about 50 ns and the error of timing deduced by the rising edge is a few tenths of a picoseconds. Eight channels of preamplifier are integrated in one PCB which is mounted close to the chamber and the ground terminal of the preamplifier is connected to the shell of the chamber to keep the noise at a low level.

3.2 DAQ hardware setup

To simplify the architecture of the electronics and DAQ, V1720 Flash-ADC digitizer modules [10] are selected to develop the system. The V1720 module is an 8-channel 12 bit sampling ADC with a sampling frequency of 250 MHz and 1.25 Msamples buffer for every channel. The dynamic range of the ADC is ±1 Vpp. The hardware structure layout of the DAQ system is shown in Fig. 3.

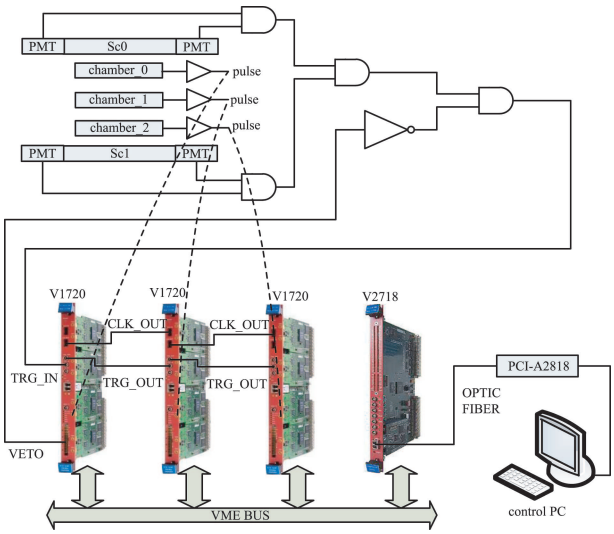

Fig. 3. (color online) Layout of the hardware structure of the DAQ system.

The hardware setup consists of VME based modules and some NIM logic units. The first digitizer board is chosen as the master board in which the sampling clock signal is generated by an on-board oscillator. The clock signal is transmitted to the post boards through the daisy chain. The boards are controlled by the V2718 controller through the VME bus. The V2718 controller is connected to the A2818 PCI board inserted in the host PC through the optical fiber. In the test setup, two scintillators are mounted on both sides of the array as the trigger detectors. Once a particle is incident, the light generated in the scintillator is collected through the light guide and detected by the PMTs at both terminals of the scintillator. The coincidence signal of the four PMTs is generated as the trigger which is sent to the input terminal of the master. The trigger signal is also transmitted to the post boards through a daisy chain. During the

procedure of data reading from the buffer of boards to the host PC, if a new trigger arrives, the event sequence may be disordered, which causes the event synchronization to be confused. To resolve this problem, a VETO signal is generated via the programmable I/O terminal and sent as an anti-coincidence with the trigger signal.

3.3 DAQ program setup

The DAQ system program was written in C, based on the Flash-ADC digitizer library and runs on Linux operating system. The block diagram of the program is shown in Fig. 4. First, the digitizer boards are activated and then the sampling parameters of the boards are configured, such as sampling length, pre-trigger ratio, threshold of channels and so on.

After the sampling configuration, the VETO signal is set to 1 to avoid a mis-trigger before the trigger is configured. In the trigger configuration step, the external trigger (Ex-trigger) is inhibited and then the system starting mode is set as started by the trigger. Then the system is triggered by a software trigger (SW-trigger) and starts to run. Because the trigger is transmitted through a daisy chain, the trigger signal sent to every board has a delay of about 40 ns relative to the previous board, so every board has a starting-delay time which makes sure that every board can start synchronously. After the system starts, the Ex-trigger is enabled and the system will be triggered by the incident particles. The system works in an interrupt request (IRQ) mode. When the IRQ waiting time is longer than the timeout limit, the system turns to the timeout procedure and the interrupt is rearmed and a new IRQ loop begins. If the system is triggered by an Ex-trigger, the master generates an interrupt requirement. At the same time the VETO is set to 1 and the data stored in the V1720 buffer are read and saved in the host PC. Once the reading ends, the IRQ is rearmed and the VETO is set to 0 and the next IRQ loop continues.

3.4 Synchronization of different boards

Because the sampling clock signal of the slave board is transmitted from the master board, generally the clock signals of different boards are not synchronized in phase. As shown in Fig. 5, the slave clock has a delay relative to the master signal.

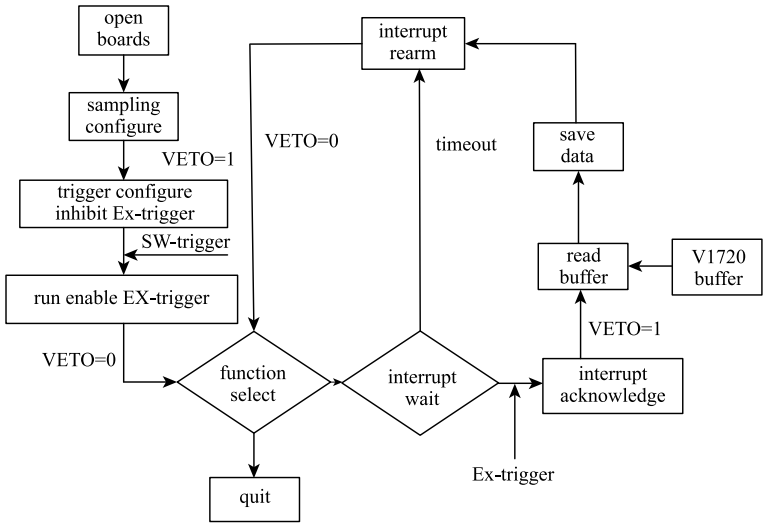

Fig. 4. The layout of DAQ program.

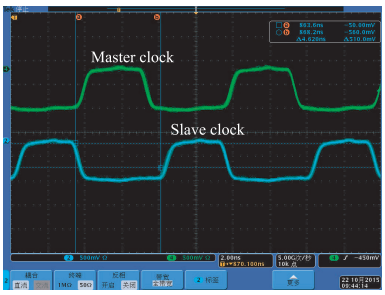

Fig. 5. (color online) The unsynchronized master and slave clock signals.

Because of the firmware structure of the trigger circuit, if the clock is unsynchronized, the trigger time tag will have a walk of two trigger periods (16 ns), as shown in Fig. 6, which will cause a large timing error. For precise timing, it is necessary to synchronize the clocks of all the boards. With the CAENUpgrader program, the phase lock loop (PLL) parameters of every board can be configured and the delay of the output clock signal can be set. After setting the PLL , the clock signals of different boards can be synchronized, as shown in Fig. 7, and the trigger time walking is reduced as shown in Fig. 8. The

main peak of the trigger time distribution has a RMS of 128 ps, which satisfies the requirement of precise timing.

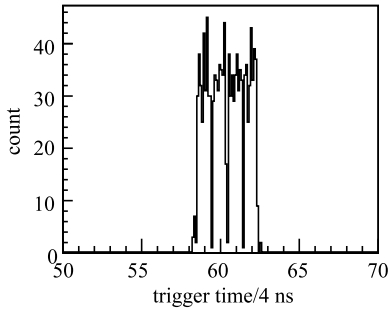

Fig. 6. The trigger time tag walking.

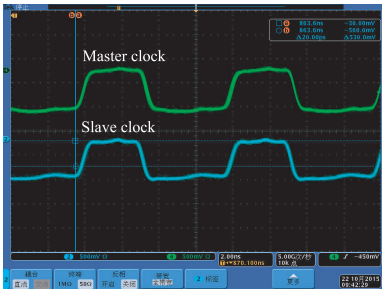

Fig. 7. (color online) The synchronized clock signal of master and slave.

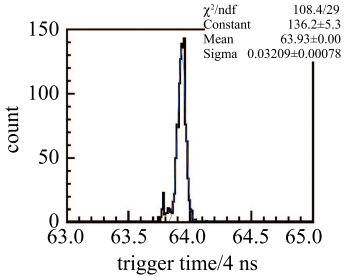

Fig. 8. (color online) The trigger time distribution after the clock synchronization.

3.5 ADC non-linearity

For the Flash-ADC digitizer, the non-linearity is one of the important properties which influences the energy resolution and timing precision. The non-linearity includes differential non-linearity (DNL) and integral non-linearity (INL). The DNL determines the ability to measure the two amplitudes with adjacent ADC output code. The INL determines the maximum deviation between the measured value and the real value of the amplitude in the full dynamic range. To test the non-linearity of the ADC, a method of histogram code density test used in Ref. [11] is chosen. A triangular waveform of amplitude of 2.2 Vpp, equivalent to 1.2 times the dynamic range of the ADC, is sent to the board. All the sampled values of the output wave are filled in a histogram which has 2^{12-2} bins and ranges from 1 to 2^{12-1}. Then the DNL of every bin is calculated using the following equation [11]:

$$DNL_i = \frac{(2^n-2)N_i}{\sum_{i=1}^{2^n-2} N_i} - 1. \quad (1)$$

In Eq. (1), N_i is the count in the i-th bin, and n is the number of ADC bits. The DNL of the ADC is shown in Fig. 9.

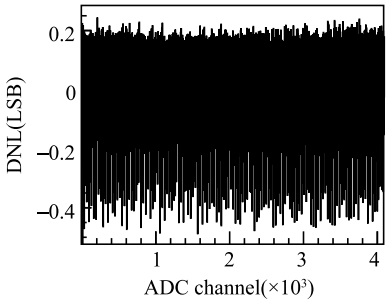

Fig. 9. The DNL histogram of the V1720 ADC.

From the histogram it is evident that the largest DNL value exceeds −0.4 LSB. The INL is calculated as [11]:

$$INL_i = \sum_{k=1}^{i} DNL_k. \quad (2)$$

The INL histogram is shown in Fig. 10. In the INL histogram, the largest deviation value exceeds 2 LSB. For gas detectors such as drift chambers which do not need a high energy resolution, the application requirements are satisfied.

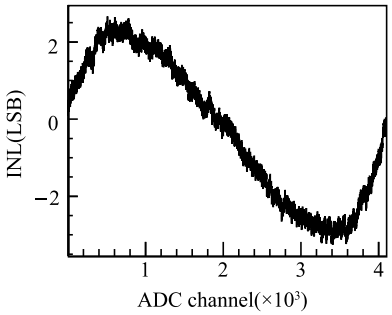

Fig. 10. The INL histogram of V1720 ADC.

3.6 The ADC ENOB

The effective number of bits (ENOB) is another important property of an ADC. Generally, because of noise and disturbance in the ADC circuit, the real resolution of ADC can't reach the ideal value and the ENOB is lower than the number of ADC bits. The ENOB is measured using the normal sine-wave fitting method [11]. A sine-wave of amplitude of 1.9 Vpp is sent to the board, the

output wave is fitted with a sine function, and the RMS of the fitting is obtained to evaluate the ENOB using the following equation [12]:

$$ENOB = n - \log_2(RMS \cdot \sqrt{12}). \quad (3)$$

In the test, one thousand sine-wave events are acquired and the fittings are processed. The χ^2 value of each fitting is filled in a histogram as shown in Fig. 11. From the histogram the average value of χ^2 can be deduced and the RMS value can be calculated. According to the measured RMS value, the ENOB of the ADC is deduced as 10.0 bits, which is a normal level of ADC performance.

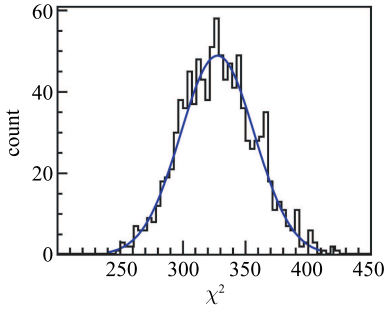

Fig. 11. The χ^2 distribution of the sine-wave fitting.

4 Digital signal processing

The acquired waveform data are stored as raw binary format. Before further analysis of track reconstruction, the digital signal processing should be done to identify real signal and filter the noise superposed on the signal. Although some noise suppression measures have been taken during the test, some random noise from the environment still exceeds the acquisition threshold and is stored. Fig. 12 shows a typical noise signal acquired in the test.

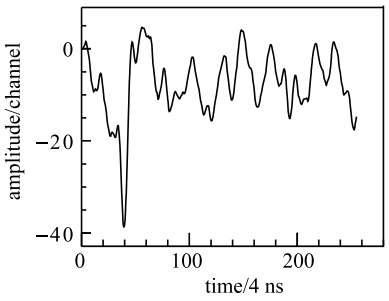

Fig. 12. Typical noise waveform acquired in the test.

It is evident that the noise signal does not have a regular shape and the amplitude is smaller than 50 mV, so the noise signal can be identified from the shape of the waveform. Because of the DC offset of the Flash-ADC, the baseline of the original waveform is not restored to zero, as shown in Fig. 13 (up), so a baseline restoring algorithm is needed. The noise superposed on the signal reduces the SNR and may affect the time and energy resolution.

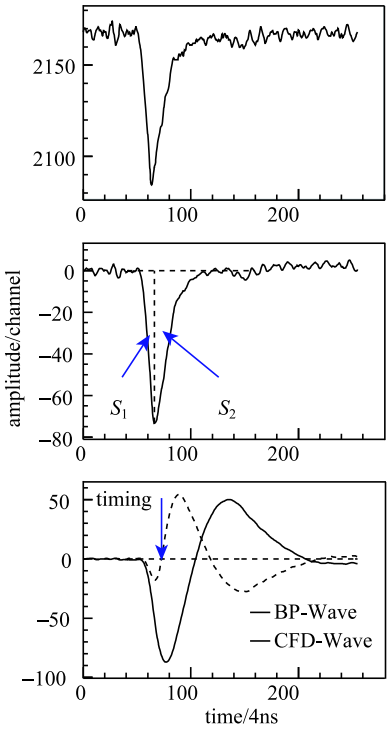

Fig. 13. (up) The original waveform has a DC offset and is superposed by noise. (mid) The waveform after the baseline restoring and the definition of pre-peak and after-peak area. (down) The BP-filter output waveform and the CFD waveform. The zero-crossing point is deduced as the timing point of the signal.

There are several widely used digital filter algorithms such as the Least Squares Method [13], Low-Pass filter [14] and Trapezoidal filter [15]. An analog active band-pass filter circuit is chosen as the model to derive the digital filter algorithm. The first part of the circuit is an RC-CR shaping net which has the functions of primary noise filtering and baseline restoring. The second part of the circuit is an active Band-Pass filter (BP-filter) which can filter the high frequency noise. The RC-CR net output waveform is shown in Fig. 13 (mid). It is evident that the baseline of the waveform has been restored to zero. Because of the RC circuit in the net, the SNR has increased a little but the noise is still reserved. With the waveform processed by the net, the ratio of pre-peak and after-peak area R can be calculated as $R = S_2/(S_1 + S_2)$, where S_1 and S_2 are the pre-peak and after-peak area respectively. The correlation distribution of R and amplitude is drawn in Fig. 14 after the total signal waveform is processed. In the plot the red rectangle regions corresponding to large (> 0.8) or small (< 0.4) R value and small amplitude (< 70 mV) represent

the noise signals which are clearly identified. So during the signal processing, thresholds are set and the signals with the parameters of over the threshold are treated as the noise.

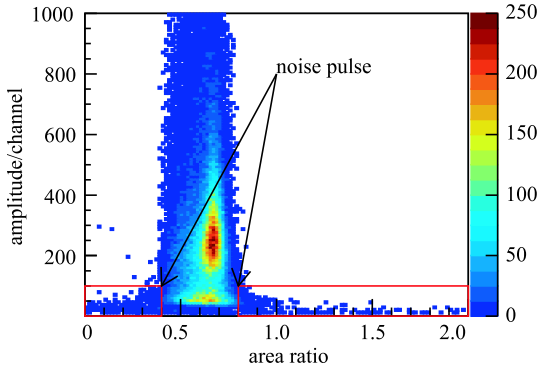

Fig. 14. (color online) The correlation distribution of R and amplitude of signals.

The BP-filter output waveform is shown in Fig. 13 (down), exhibiting a bipolar feature caused by the phase-frequency property of the filter. For the BP-filter output waveform, the minimum value of the first peak is obtained as the amplitude of the signal. The arrival time of the signal is derived from the digital CFD method [12]. The CFD waveform is drawn with the dotted curve in the Fig. 13 (down), and the first zero-crossing point is treated as the timing point of the signal. A linear interpolation method is used to deduce the crossing time.

5 Some primary results of beam test

In the beam test, the beam perpendicularly bombards on the detector array and thus the time of flight can be measured with the scintillator TOF detector. The working high voltages of the PMTs are calibrated to 700 V, 700 V, 770 V and 680 V to make sure every PMT has a similar gain and counting rate. The measured TOF distribution is shown in Fig. 15.

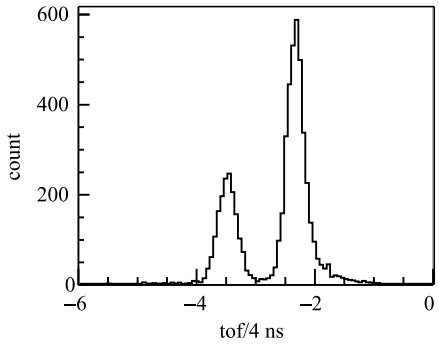

Fig. 15. The TOF distribution in the beam test. The two peaks correspond to pions (left) and protons (right) respectively. The zero point of timing has not been calibrated in this histogram.

Because the particles in the beam have the same momentum, from the histogram it is evident that there are two components in the beam. The left peak corresponding to a short TOF with a higher speed is contributed by pion, and the right peak is contributed by proton. From the TOF distribution, the time resolution of 600 ps can be obtained by fitting the peak. This resolution can satisfy the requirement of the application.

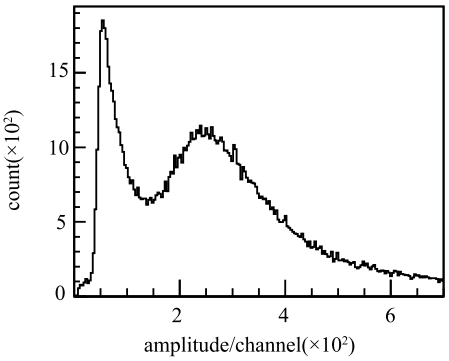

Fig. 16. The energy loss distribution of a single wire.

The energy loss distribution of a single wire is shown in Fig. 16. The particle loses a little energy in a single wire cell because of the thin gas layer which causes a large statistical fluctuation so the energy distribution has a large broadening. The Landau tail of the distribution further reduces the resolution. To get a better energy resolution, it is necessary to add the total energy loss of fired wires after the gain of every wire is calibrated. The drift time distribution is plotted in Fig. 17. The width of the main distribution region is about 200 ns, corresponding to an electron drift velocity of about 5 cm/μs, which is a typical value of the gas component filled in the chamber.

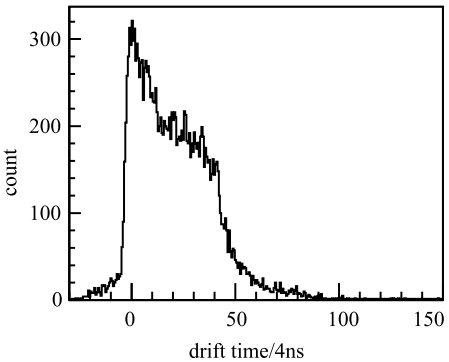

Fig. 17. The typical drift time distribution of a single wire.

The distribution has a sharp leading edge and trailing edge which corresponds to the center and boundary of the wire cell respectively. The counts before the leading edge are contributed by the background and the long tail is contributed by the electrons ionized in the corner of the cell where a long drift time is expected.

6 Summary

A large size prototype of the drift chamber array for the External-Target-Experiment at HIRFL-CSR has been made. A DAQ system based on Flash-ADC modules has been developed and tested. The performance of the electronics and the DAQ system match the requirement of the detector test. The prototype array has been tested at the IHEP E3-Line with a beam of pions and protons. The acquired waveforms have been processed with the digital signal processing algorithm to identify the noise and increase the SNR. A digital CFD timing method is used to determine the arrival time of the signal. The TOF distribution and drift time distribution are obtained, showing that the whole integrated system functions properly. Further data analysis should be focused on the track reconstruction, the detector array alignment and the calibration of space-time relation of electron drifting.

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