A digital low-level radio-frequency system R&D for a 1.3 GHz nine-cell cavity

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Abstract: To test and verify the performance of the digital low-level radio-frequency (LLRF) and tuner system designed by the IHEP RF group, an experimental platform with a retired KEK 1.3 GHz nine-cell cavity is set up. A radio-frequency (RF) field is established successfully in the cavity and the frequency of the cavity is locked by the tuner in $\pm 0.5^\circ$ (about ± 1.2 kHz) at room temperature. The digital LLRF system performs well in a five-hour experiment, and the results show that the system achieves field stability at amplitude <0.1% (peak to peak) and phase $<0.1^\circ$ (peak to peak). This index satisfies the requirements of the International Linear Collider (ILC), and this paper describes this closed-loop experiment of the LLRF system.

Key words: LLRF, tuner, 1.3 GHz, RF, ILC

PACS: 29.20.Ej, 07.57.Kp **DOI:** 10.1088/1674-1137/36/3/013

1 Introduction

The amplitude and phase stability of the RF field directly affects the quality of the beam in accelerators. The ILC [1] requires an RF amplitude stability of $\pm 0.1\%$ and phase stability of $\pm 0.1^\circ$, and the LLRF system is the core equipment used in modern accelerators to maintain the high-precision RF field.

A digital LLRF system has been designed by the RF group at IHEP to study the ILC LLRF system, and an experimental platform has been set up at room temperature at a retired KEK 1.3 GHz nine-cell cavity MHI-04 to test the performance of the system. The results show that the system, which is based on an special IQ detection algorithm, can achieve field stability at amplitude <0.1% (peak to peak) and phase $<0.1^\circ$ (peak to peak) in five-hour closed-loop experiments. This specification meets the requirements of the ILC. The IQ detection algorithm and the closed-loop experiment will be described in this paper.

The experimental platform is a mini RF system consisting of the cavity, the tuner, the LLRF subsystem, an interlock system and some RF equipment. The frame diagram is shown in Fig. 1.

A precise RF signal from an Agilent signal source is sent to an in-phase and quadrature (IQ) modulator. After being amplified by a 42 dB RF amplifier, the signal is coupled into a cavity with a high-power coupler. The RF field of the cavity is disturbed by bead pulling, and the disturbed RF wave is picked up by antennas and then fed into a digital LLRF cabinet. The cabinet down-converts the RF signal to an intermediate frequency (IF) signal first, and then a field programmable gate array (FPGA) board, which is the core component of the cabinet, processes the IF

Table 1. The main index of the RF system.

parameter	value
power of pickup signal	20 dBm
coupling parameter (β)	0.38
intrinsic quality factor(Q_0)	8000
loaded quality factor ($Q_{\rm L}$)	5800
bandwidth	220 kHz
radio frequency	1297.545 MHz
intermediate frequency	3 MHz

Received 2 June 2011

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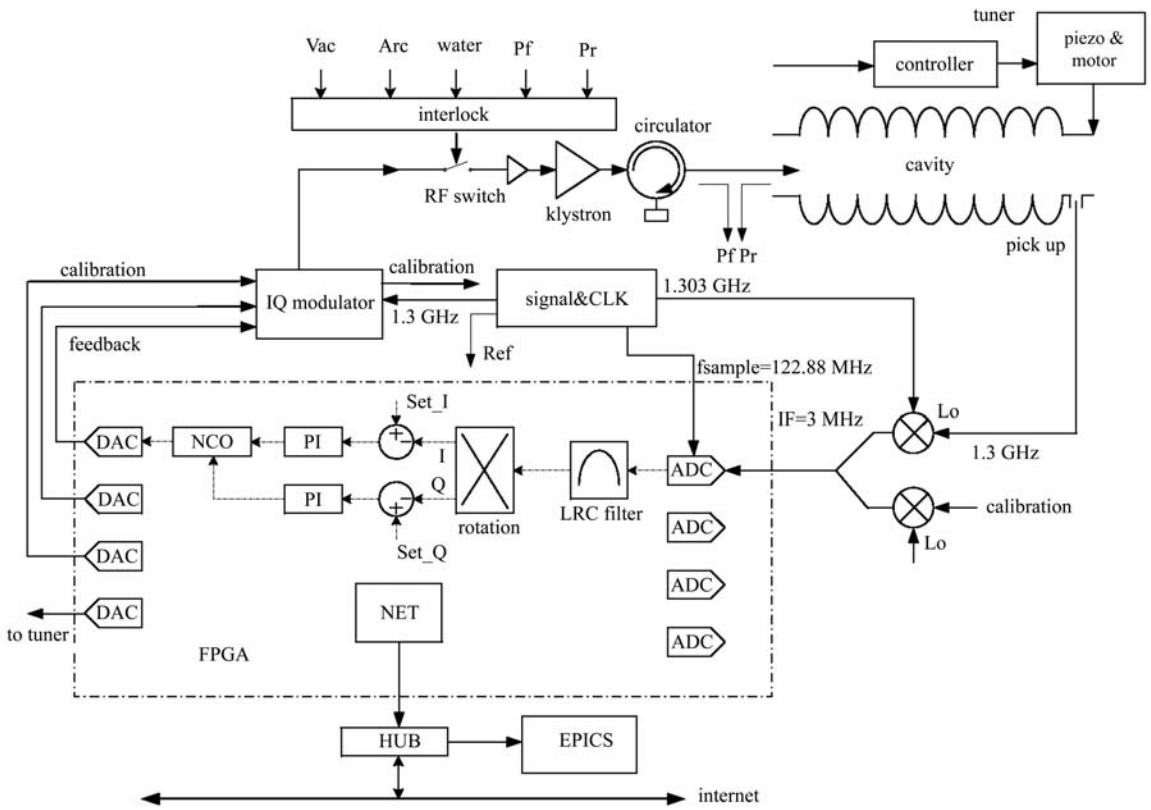

Fig. 1. Overview of the digital LLRF system for the 1.3 GHz nine-cell cavity.

signal, Finally, the useful information is sent to the IQ modulator and the tuner to control the amplitude, phase and frequency loops. The main index of the RF system is shown in Table 1.

2 The LLRF system

The LLRF system consists of several subsystems, including the signal and clock subsystem, the RF front-end and back-end model, the AD/DA and FPGA board, the calibration system, and the communication subsystem. Several chief parts are introduced as follows.

2.1 Signal and clock

A flexible signal & clock subsystem is designed in our LLRF system. The main advantage of the system is the frequency of the Lo signal, the IF signal, and that the sampling clock can be changed in a certain range. A unique IQ detection method with an arbitrary $f_{\rm IF}/f_{\rm sample}$ rate is selected to demodulate the IQ signal; this will be introduced later in this paper. The structure of the signal and the clock and the frequency of all the main signals are given in Fig. 2.

The 1.3 GHz RF signal is generated by a master oscillator (MO). The output of two direct digital synthesizers (DDS) AD9912, featuring a 1GSPS 14 bit DAC, is mixed with the RF signal. Then the frequency of the Lo signal can be modified by adjusting the output of the PLL (phase locking loop) AD9912. The 122.88 MHz sampling clock for AD/DA is supplied by the voltage control X-tal crystal oscillator (VCXO) embedded in the AD9510. All these signals are locked with the main signal source to keep synchronization. The test shows that each signal and clock meets the requirements of the original design.

2.2 Digital board

A latest generation FPGA board 4SGX230 from Altera is used to establish our LLRF system. The digital board is connected with two 14 bit AD/DA daughter boards with a high speed mezzanine card (HSMC). The highest sampling rates of the ADC and DAC are 150 and 250 Mbps, respectively.

Feedback control and interlock protection are accomplished by the FPGA board. Besides, the FPGA board communicates with the PC by TCP/IP protocol with an embedded real-time operating system. A specialized Labview procedure is used to read/write the data.

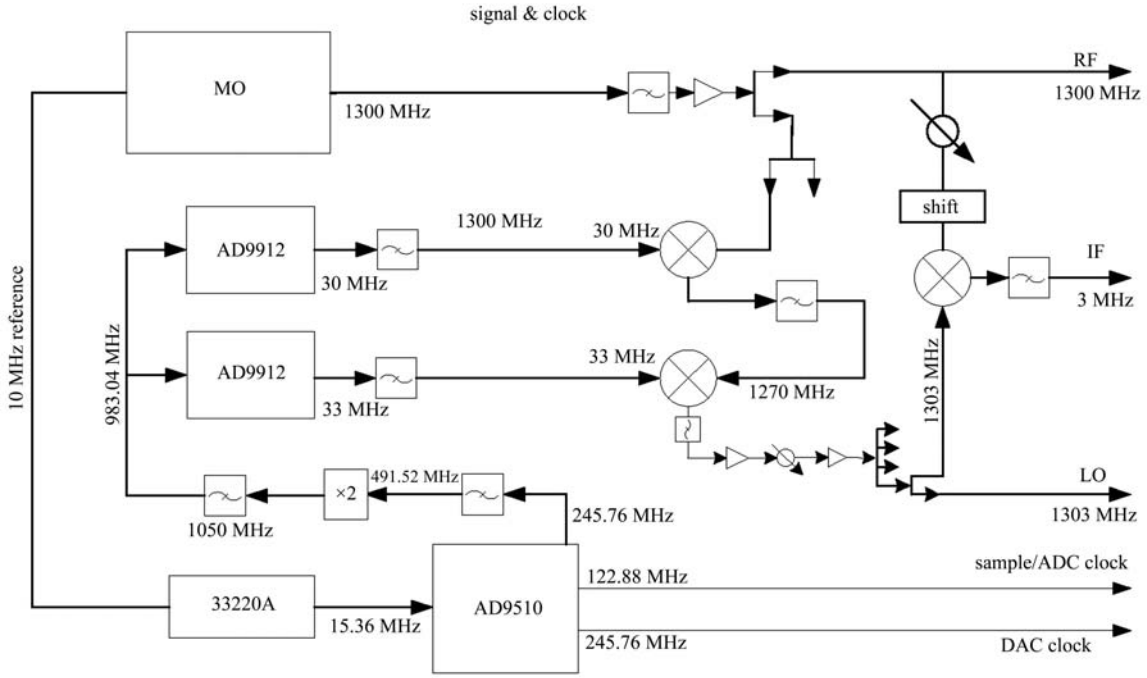

Fig. 2. Layout of the signal and clock subsystem.

2.3 RF front-end and back-end model

Four RF signals are down-converted in the RF front end: the reference signal comes from the signal source, the forward signal which is fed into the nine-cell cavity, the reflection signal reflected from the nine-cell cavity, and the signal picked up from the cavity. These four signals are used for field control and Tuner control.

In the RF back-end, two 30 MHz signals which carry the useful amplitude and phase information are generated by DDS in the FPGA board. They are up-converted to RF signals. An appropriate surface acoustic wave (SAW) filter and other RF devices are selected for a dynamic of more than 20 dB.

The LLRF control box consists of three layers (Fig. 3):

Fig. 3. The layers of the LLRF control box.

the bottom layer is the power supply model and the FPGA board, the middle layer and the boards suspended in the two sides of the box are used for generating a group of synchronized signals and the clock, and the analog front-end is placed on the top layer.

2.4 Communication system

The communication system consist of two subsystems: the first one is in charge of the communication between the local computer and various measuring instruments. The instruments are connected in series with a general purpose interface bus (GPIB). Each instrument has an independent address. A Labview procedure accesses each instrument with an NI PCI-GPIB data acquisition (DAQ) card by polling. The second subsystem manages the communication between the local computer and the remote computer. With the help of the experimental physics and industrial control system (EPICS) server provided by Labview, the data collected by the DAQ card are converted to processing variables, and therefore the whole system is embedded in the EPICS environment. Furthermore, several EPICS clients in the different computers can be connected together with the Ethernet to realize the distributed control.

3 Algorithm

Algorithms are the core of a digital LLRF system.

Some new algorithms are involved or attempted in our system.

3.1 IQ detection

The determination of how to demodulate the high-precision IQ signal is the basis for high-precision RF control. At present, the methods based on IQ and non-IQ sampling are the most well rounded and widely used [2, 3].

The IQ sampling technique samples the IF signal every 90° (or 270°, or 450°$\cdots$(2n−1)×90°). This method is simple and easy to understand, but the nonlinearities of ADC are serious [4]. A non-IQ method proposed by Doctor Larry Doolittle suppresses the nonlinearities successfully. However, the non-IQ method needs a carefully selected ratio of the IF to the sample clock.

We introduce a special algorithm in IQ detection; compared with the method based on IQ sampling or non-IQ sampling. Our method does not need a strict ratio of the IF to the sample clock. That is to say, under the principle of Nyquist's sampling theorem, we can obtain the high-precision IQ signals with an arbitrary $f_{\rm IF}/f_{\rm sample}$ rate. This method is based on a rotation algorithm, which is illustrated in Fig. 4.

As shown in Fig. 4, the (I_0, Q_0) is the IQ signal we need. If the (I_n, Q_n) is known, then the IQ signal can be obtained by multiplying the β with a rotation gene $\mathrm{e}^{-\mathrm{j}\omega_0 n}$, and the process is expressed by Eq. (1).

$$\begin{pmatrix} I_0 \\ Q_0 \end{pmatrix} = \begin{pmatrix} \cos\omega_0 n & -\sin\omega_0 n \\ \sin\omega_0 n & \cos\omega_0 n \end{pmatrix} \cdot \begin{pmatrix} I_n \\ Q_n \end{pmatrix},$$
$$\omega_0 = \Omega_0 T, \tag{1}$$

where Ω_0 is the resonant frequency and T is the period of the sampling signal. The (I_n, Q_n) signal can be acquired with the help of a special infinite impulse response (IIR) filter, which is based on an analog resistance, inductance, capacitance (RLC) resonant circuit.

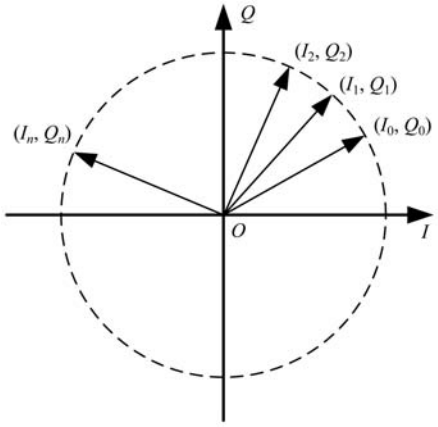

Fig. 4. The IQ and IF signals under IQ coordination.

The RLC resonant circuit has good frequency-selective properties which can be used for filter design. After some mathematical treatments of the transfer function of the RLC circuits [5], the discrete impulse response function of the circuit in plural form can be simplified as:

$$h(n) = \mathrm{e}^{-\alpha T + \mathrm{j}\omega_0 n},\ \alpha = \frac{\Omega_0}{2Q},\ \omega_0 = \Omega_0 T. \tag{2}$$

This is an IIR filter, and the bandwidth of the filter depends on the value of Q. According to the residue theorem [6, 7], the output of the IIR filter $y(n)$, which is the convolution of the discrete IF signal and the filter $h(n)$, can be calculated by $Y(z)$, the

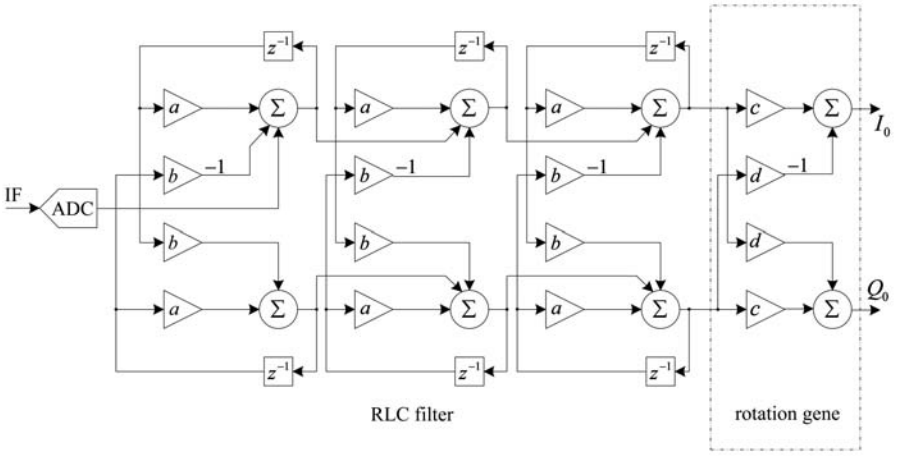

Fig. 5. The structure of a triple-order RLC filter group and the IQ detection method. Parameters a and b can be obtained by Eq. (2): $a = \mathrm{e}^{-\alpha T}\cos\omega_0$, and $b = \mathrm{e}^{-\alpha T}\sin\omega_0$. The parameters of c and d depend on Eq. (1), which is $c = \cos\omega_0 n$ and $d = \sin\omega_0 n$.

z-transform of $y(n)$. It can be proven that (I_n, Q_n) is only involved in the expression of $y(n)$. It is also easy to verify that the cascade filter group will improve the performance greatly. The structure of the filter and the integrated IQ detection method is illustrated in Fig. 5.

3.2 Other algorithms and technologies

Some other beneficial attempts and approaches are tried in our system. They are:

1) The ROM compression algorithm in DDS. To reduce the spurious signal in DDS, we tried many compression methods and got remarkable results [8]. The modified DDS algorithm improved the spurious free dynamic range (SFDR) by 15 dBc.

2) Temperature calibration technology. Temperature drift is a common phenomenon in RF devices and limits the stability of the RF field. Temperature calibration technology provides a method to eliminate the drift [9]. A calibration interface is reserved in our system. Further experiments will be done to validate the correctness of this method.

4 Results

4.1 The frequency loop experiment

The nine-cell cavity has a small Q value and wide bandwidth at room temperature. When the speed of the bead controlled by a bead-pulling motor is too high, the main motor connected to the tuner cannot follow the pace of the bead, so we limit the speed of bead to 0.06 mm/s. Meanwhile, we only let the bead move around in the 1# cavity. This process can be illustrated in Fig. 6(a). At the beginning, the system is operated in an open loop (the tuner does not work), and the phase difference between the forward signal and the pick-up signal varies according to the position of the bead. Then the loop is closed at time $t1$, and the phase difference can be locked to $\pm 1^\circ$ by the tuner. Finally, we can limit the phase difference to $\pm 0.5^\circ$ (about ± 1.2 kHz) when the bead-pulling motor is stopped at time $t2$.

4.2 The amplitude and phase loop experiment

A proportional-integral (PI) controller embedded in the FPGA board is used to control the amplitude and phase. When the loops are settled, the amplitude and phase are locked at the set value. The control precision is shown in Fig. 6(b), (c). The fluctuation of the field is less than $\pm 0.1\%$ (peak to peak) in amplitude and $\pm 0.1^\circ$ (peak to peak) in phase in 5 h. The details are shown in Table 2.

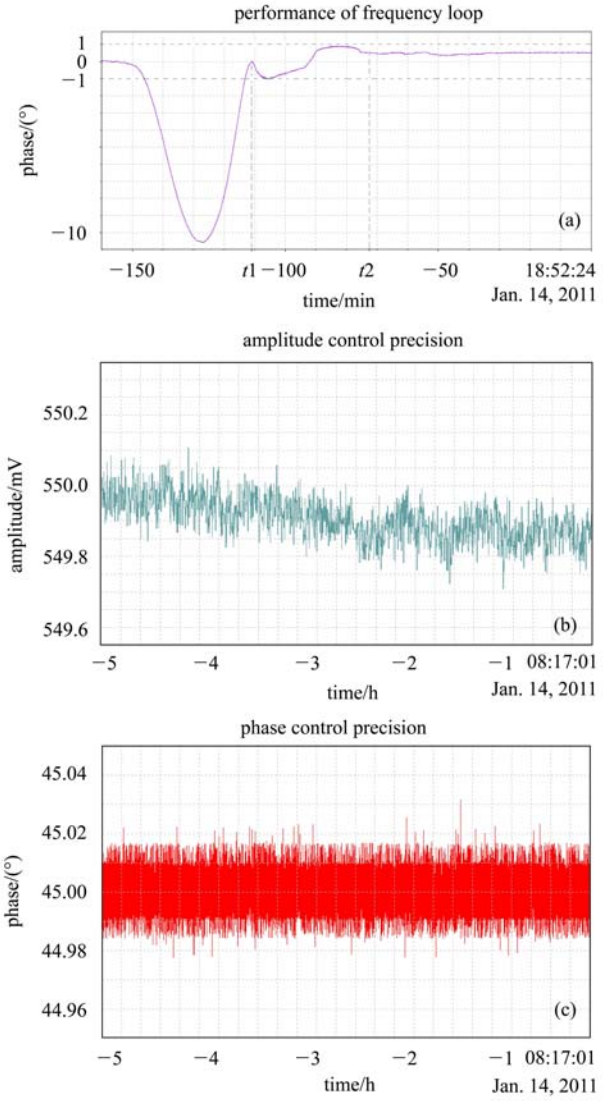

Fig. 6. (a) The performance of the frequency loop. The tuner is activated at time $t1$ and the switch of the bead-pulling motor is turned off at time $t2$. (b) Amplitude control precision in 5 h. (c) Phase control precision in 5 h.

Table 2. LLRF performance summary.

parameter	index
operation mode	CW
frequency loop	± 1 kHz in room temperature
amplitude loop	$< \pm 0.1\%$(peak to peak)
phase loop	$< \pm 0.1^\circ$(peak to peak)
settle time	100 μs
dynamic range	20 dB

4.3 Experimental problems

Control precision decreases when the temperature of some of the RF devices becomes too high. This will be improved in our next LLRF control box.

5 Summary

The IHEP 1.3 GHz digital LLRF system R&D performs well. We tried some new methods and have gained some initial success. The five-hour closed-loop results show that the amplitude error is smaller than 0.1% and the phase noise is less than 0.1°. Some other new methods and algorithms in LLRF will be attempted in our system, and furthermore a liquid nitrogen or liquid helium test will be done in future to validate this system in the 2 to 4 K environment.

Many thanks to the beneficial discussions with Doctor Larry Doolittle from the Lawrence Berkeley Accelerator Lab.

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