A comparison study of on-chip short pulse generation circuits based on a coplanar waveguide

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Abstract: A few traditional pulse-forming circuits are implemented in a commercial 0.13 μm digital complementary-metal-oxide-semiconductor (CMOS) technology. These circuits, based on a coplanar waveguide, are analyzed and compared through Cadence^{TM} Spectre simulations. The results show that these traditional pulse-forming-line (PFL) based circuits can be implemented in standard CMOS technology for short pulse generations. Further work is needed to explore the potential of the circuit techniques and to minimize parasitic effects.

Key words: pulse generation circuit, transmission line, PFL, CMOS, coplanar waveguide

PACS: 84.30.Ng, 84.30.Sk, 42.70.Nq **DOI:** 10.1088/1674-1137/35/3/012

1 Introduction

Pulse-forming-line (PFL) based on-chip pulse generation circuits are promising to extend the high-speed short-pulse generation capabilities of standard complementary-metal-oxide-semiconductor (CMOS) devices and circuits. They are also promising to generate high voltage and high power electrical pulses on-chip for high performance system-on-chip (SOC) development. Therefore, it is of great interest to explore the functionality and applicability of various PFL-based circuit architectures, which were originally developed in the pulsed-power community, in standard digital CMOS technologies.

Unique characteristics and challenges of CMOS technology for on-chip pulse generation include multilayer, yet lossy, interconnected resources for PFL realization, very limited chip area (since the largest die size is about 1.5 cm×1.5 cm), low operating voltage (∼1 V voltage supply, due to reliability considerations) and the proximity of other circuit components (i.e. potentially strong electromagnetic interference). Furthermore, electro-migration, which is not an issue in conventional pulsed-power technologies, sets an upper limit on current density.

Compared with other TLs, the coplanar waveguide (CPW) provides higher operating frequencies, better control of line characteristics and field shielding capabilities, which are desirable in order to minimize crosstalk and noise. Also, the signal line and ground line of the CPW are in the same layer, which makes on-chip fabrication much easier. As a result, on-chip CPWs have attracted a lot of attention.

In this work, we compare the performance and limitations of a few conventional pulse forming circuits in a commercial 0.13 μm digital CMOS technology. Through Cadence^{TM} Spectre simulation with extracted circuits from layout, we investigate the implications of the issues mentioned above. Standard devices provided by the process vendor are used for simulation evaluations.

2 Typical PFL-based pulse generation circuits

PFL is a common circuit approach for short pulse generation [1, 2] in pulsed-power technologies, because PFLs can store an exact amount of energy and discharge the energy into the load with a specified pulse shape. At the same time, pulse compression is achieved to obtain a high voltage output from a low voltage supply.

A basic PFL-based pulse generation circuit is shown in Fig. 1 (hereafter referred to as circuit A). It operates as the following: the transmission line (PFL)

Received 8 June 2010

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is first slowly charged to voltage V_0. After the switch closes, an output pulse, $V_{\rm out}$, is formed when $R_{\rm load} = Z_0$ (matching condition) with amplitude of $\sim V_0/2$ and a pulse duration that is determined by the length of the transmission line, $\tau \approx 2d/v$, where v is the local speed of light and d is the transmission line length. The turn on time of the switch $T_{\rm on}$ determines the rise edge of the generated pulse. In order to obtain better switch performance, the circuit is grounded between the switch and the load resistor. Therefore, a negative output pulse is obtained. The circuit performance will be used in this work for comparison.

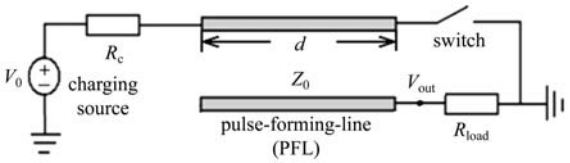

Fig. 1. Basic pulse generation circuit with a PFL (circuit A).

Figure 2 shows the schematics of the circuits that will be compared in this work. Fig. 2(a) circuit B shows the Blumlein PFL pulse generator [3], in which two identical PFLs are connected in series with a load resistor. Compared with the circuit A in Fig. 1, the Blumlein PFLs double the load voltage. Therefore, the output pulse amplitude is V_0, the power supply voltage. Fig. 2(b) circuit C shows a bipolar pulse generator. Unlike the typical circuit A in Fig. 1, the switch is connected at the front end of the PFL. When the switch closes, the front end is in short condition. A bipolar pulse with an amplitude of $V_0/2$ will be obtained. Fig. 2(c) circuit D shows a pulse generator with a single PFL, in which the output is connected to its input in parallel [4]. After switching, the discharging process of the PFL capacitors starts simultaneously from both the input and output ports. Thus, the output pulse duration is reduced by a factor of two when compared with the circuit in Fig. 1. Fig. 2(d) circuit E [5] is similar to the bipolar pulse generator (i.e. circuit C) but one additional matching

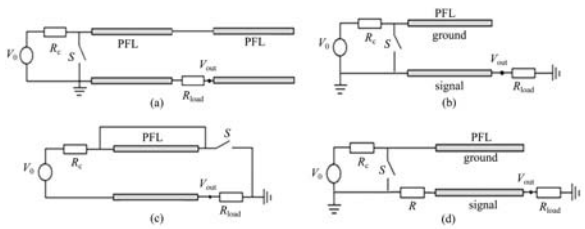

Fig. 2. Different pulse generation circuits with PFLs. (a) circuit B: Blumlein; (b) circuit C: Bipolar pulse generation; (c) circuit D; (d) circuit E.

resistor, $R = Z_0$, is added at the input terminal of the PFL. Therefore, no reflection occurs at this end. For all those circuits mentioned above, due to the same reason as circuit A, we ground the right side of the switch. Therefore, the output pulses are negative, and for circuit C, the bipolar pulse circuit, the negative pulse happens prior to the positive one.

Table 1 summarizes the main output parameters of the PFL based circuits in which d is the PFL length, v is the local speed of light and V_0 is the power supply voltage, Z_0 is the characteristic impedance of PFL.

Table 1. Ideal output pulse parameters of the circuits in Figs. 1 and 2.

circuit	pulse duration	pulse amplitude	matching condition
A	$2d/v$	$-V_0/2$	$R_{\rm load} = Z_0$
B	$2d/v$	$-V_0$	$R_{\rm load} = 2Z_0$
C	d/v	$mV_0/2$	$R_{\rm load} = Z_0$
D	d/v	$-V_0/2$	$R_{\rm load} = 0.5Z_0$
E	d/v	$-V_0/2$	$R_{\rm load} = R = Z_0$

3 Simulation analysis of CPW-based pulse generation circuits

The commercial IBM CMOS 8RF_DM 0.13 μm technology is used to implement these circuits discussed above. Fig. 3 shows the schematic and layout of circuit A. All circuit components are standard devices provided by the process vendor. A MOSFET is used as the switch and a meandered CPW is used

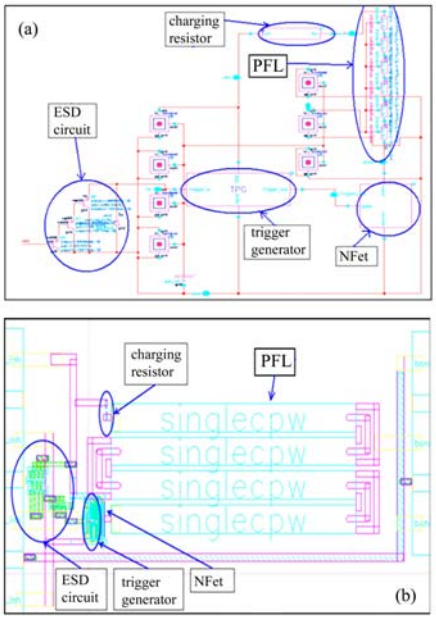

Fig. 3. (a) Schematic of circuit A. (b) Layout of circuit A.

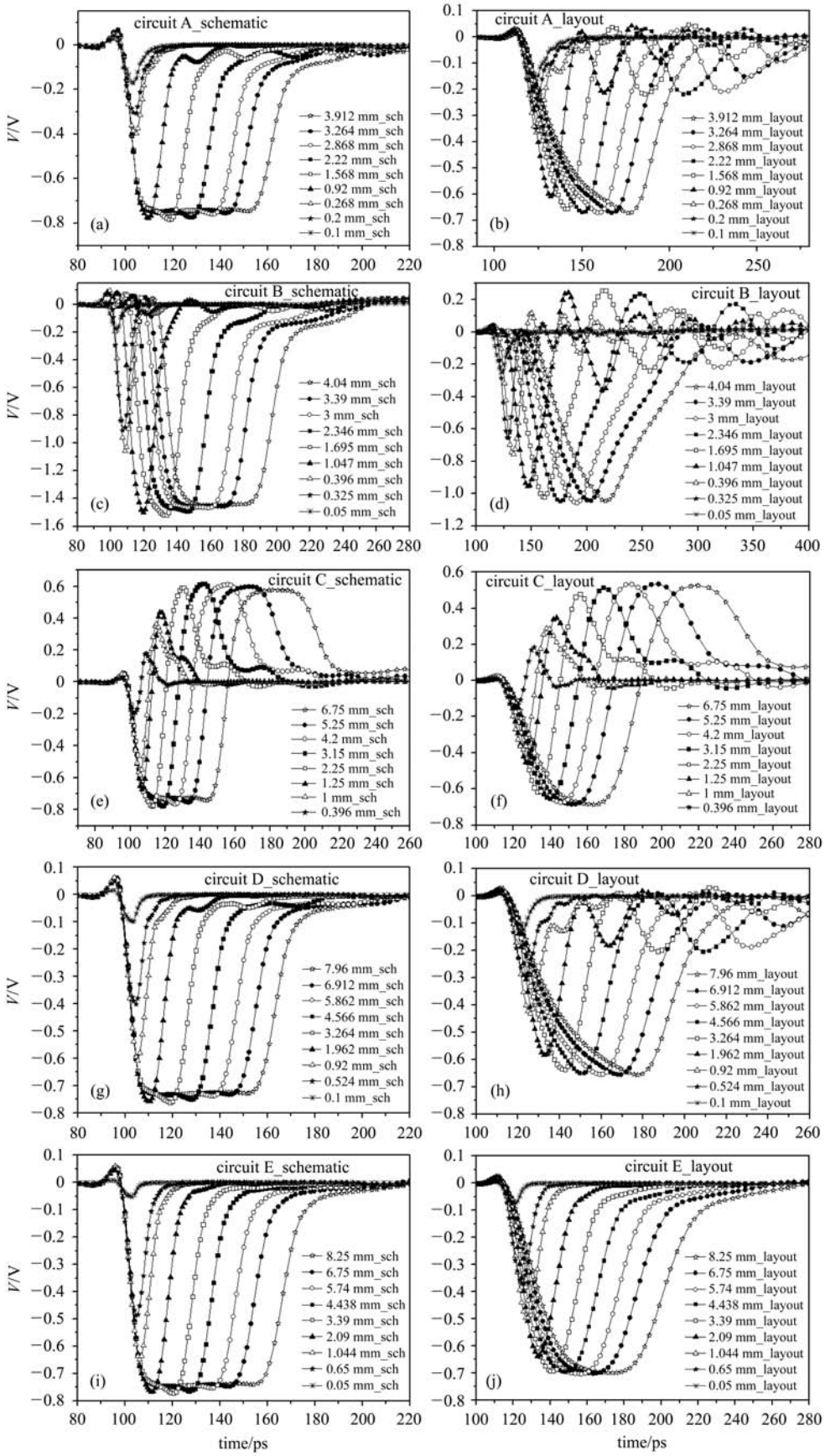

Fig. 4. Output waveforms obtained with Cadence^{TM} Spectre simulation for different PFL lengths.

as the pulse-forming-line. The input DC voltage is V_0=1.6 V, the charging resistor R_c=1.5 kΩ, the propagation velocity v along the PFL (a meandered on-chip coplanar waveguide) is about 1.3×10^8 m/s. Fig. 4 shows the simulated output pulses obtained with Cadence™ Spectre.

The results in Figs. 4 and 5 show that typical pulse generation circuits work reasonably well in CMOS technologies. As expected, the pulse duration of each circuit is determined by the CPW length. However, the amplitude of the output pulse is much less than that predicted in Table 1 when the CPW is short. Table 2 shows the shortest pulse we could obtain of each circuit and the associated biggest output voltage and associated CPW length (here we set 20% of the ideal output amplitude as the threshold). There are two main reasons for the discrepancies: the loss on the switches since their R_{on} is not 0 Ω, and the relatively long switching time (due to a finite trigger pulse rise edge, finite MOSFET speed and parasitic effects). Pulses that are much shorter than the FO4 delay of the given CMOS technology can be obtained even at lower voltage levels. Therefore, the circuit techniques extend the short-pulse generation capabilities of CMOS devices.

Table 2. The shortest pulse comparison.

circuit	simulation result in cadence™ spectre				PFL length/mm
	schematic		post-layout		
	pulse duration/ps	output voltage/V	pulse duration/ps	output voltage/V	
A	7	−0.38	8	−0.34	0.27
B	7	−0.85	8	−0.62	0.32
C	5/6	−0.20/0.17	8/9	−0.17/0.17	0.40
D	6	−0.37	8	−0.30	0.52
E	7	−0.48	10	−0.35	0.65

Compared with the schematic simulations, Fig. 4 shows that the post-layout results have longer delays, longer rise edges and longer fall edges. The rise and fall time of the generated output pulses are determined by the parasitic capacitance and resistance of the MOSFET switch, CPW and load. The post-layout results (Fig. 4 (b, d, f, h, and j)) also show that the pulse rise time increases with the increase of CPW length. Layout-related parasitic effects probably caused these CPW-length related rise times to increase, even though further work is needed to pinpoint the sources.

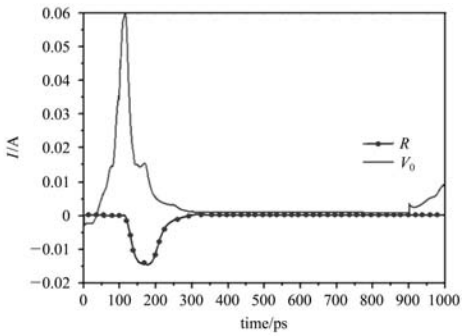

Fig. 5. Currents through source, V_0, and load R in post-layout simulation.

Figure 5 shows the currents that pass through V_0 and load in circuit E in the post-layout simulation. The currents dictate the CPW line width and other interconnection line widths due to the on-chip reliability (i.e. electro-migration) concerns.

4 Conclusions

Through simulation studies, in this work we compare the performance and limitations of typical pulse-generation circuits in a 0.13 μm digital CMOS technology. Standard devices provided by the process vendor are used in the analysis. A meandered CPW is used as the pulse-forming-line. The results show that traditional pulsed-power circuits can be exploited in integrated circuit processes for short pulse generations. Further work is needed to identify and minimize the parasitic effects.

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