FPGA-based amplitude and phase detection in DLLRF*

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Abstract The new generation particle accelerator requires a highly stable radio frequency (RF) system. The stability of the RF system is realized by the Low Level RF (LLRF) subsystem which controls the amplitude and phase of the RF signal. The detection of the RF signal's amplitude and phase is fundamental to LLRF controls. High-speed ADC (Analog to Digital Converter), DAC (Digital to Analog Converter) and FPGA (Field Programmable Gate Array) play very important roles in digital LLRF control systems. This paper describes the implementation of real-time amplitude and phase detection based of the FPGA with an analysis of the main factors that affect the detection accuracy such as jitter, algorithm's defects and non-linearity of devices, which is helpful for future work on high precision detection and control.

Key words digital LLRF, high-precision, CORDIC, amplitude and phase detection, FPGA, jitter, ADC nonlinear

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1 Introduction

With the development of particle accelerators, high RF power and high RF stability are the key features to be achieved in the RF system. LLRF is a subsystem in the RF system used to stabilize the amplitude and phase of the accelerating field. The Beijing Electron Positron Collider Upgrade (BEPC Ⅱ) requires the RF phase stability to be within $\pm1^\circ$, and the amplitude stability to be within $\pm1\%$. As a much higher requirement, the International Linear Collider (ILC[1]) and the Free Electron Laser (XFEL[2]) require RF amplitude of $\pm0.01^\circ$ and phase stability of $\pm0.01\%$.

The development of microelectronics technology has made it possible to implement LLRF digitally. High speed and high resolution ADC and DAC can easily convert the IF analog signal to digital signal and vice versa. FPGAs are capable of fast and real time complex calculation. Almost all the digital LLRF control systems use high speed ADC to sample the IF (or RF) signal and complete some fast computation in FPGA, finally recovering the IF (or RF) signal via DAC.

The detection of RF amplitude and phase is the fundamental step to realize the digital LLRF control. To achieve low-latency control, the digital LLRF control systems need to be based on a direct digital IQ method. Signals are sampled in an interval of 90° (90° or odd times of that interval) and the control loop uses IQ components separately.

Up to now, the amplitude and phase detection based on FPGA in different methods has been studied and completed. Analysis of the CORDIC algorithm and the main factors which affect the accuracy of amplitude and phase detection such as clock jitter, algorithm defect and ADC nonlinear characteristics will be described in this paper.

2 IQ detection[3]

The IQ method[4] has been commonly used in RF

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amplitude and phase detection in both analog[5] and digital LLRF control systems. A signal $x(t)$ Eq. (1) can be represented by an "In-phase" component $I(t)$ with a "Quadrature" component $Q(t)$ Eq. (2),

$$x(t) = \mathrm{Re}(A(t)\mathrm{e}^{\mathrm{j}(wt+\theta(t))}), \tag{1}$$

$$\begin{aligned} I(t) &= A(t)\cos(\theta(t)), \\ Q(t) &= A(t)\sin(\theta(t)). \end{aligned} \tag{2}$$

1) Digital IQ sampling

A digital IQ sampling method uses a super heterodyne structure (Fig. 1), high-frequency signals are down converted to intermediate frequency signals, then a relevant clock signal is chosen as the ADC sampling clock, and finally FPGA is used to calculate the amplitude and phase from the IQ sequence data.

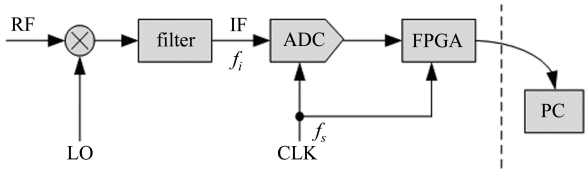

Fig. 1. The digital IQ phase detection structure.

In this method the IF signal and sampling clock meet relation $f_{\mathrm{IFsignal}}/f_{\mathrm{sampling}} = (2m-1)/4$ ($m = 2n-1, m \in N$). When $m = 1$, the signal is sampled in an interval of 90°, and the data stream (Digital IF IQ signal) can be expressed as $I/Q/-I/-Q\cdots$, and then, FPGA calculates the signal's magnitude and the phase from the obtained IQ stream.

2) Integer IF periods sampling[6] and the digital down converter method

When $f_{\mathrm{IFsignal}}/f_{\mathrm{ampling}} = 1/M$ ($4 \ll M \in N$) we can integrate using one period of the sampled IF data to average out the harmonics and get a lower noise level. The mathematic relation can be represented in Eq. (3). Fig. 2 demonstrates that the parallel hardware implementation makes M samples to one result, when the window moves with the clock we get the result for each period. For example, we can use a 100 MHz clock to sample the 1 MHz signal, which approximately makes the noise level one tenth compared with the common method[6].

$$\begin{aligned} I &= 2/M \sum_{i=0}^{m-1} x_i \sin(i \cdot \Delta\theta), \\ Q &= 2/M \sum_{i=0}^{m-1} x_i \cos(i \cdot \Delta\theta). \end{aligned} \tag{3}$$

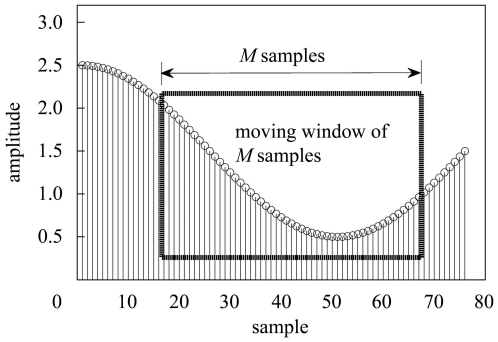

Fig. 2. Integer times sampling method.

Also we can use the DDC (digital down converter) architecture[7] to get the I and Q components and implement amplitude and phase detection (Fig. 3). This method will cost less hardware resources and need a shorter delay. The sampling rate of the DDC may be 3—5 times of the signal when the bandwidth is much lower compared with the IF signal.

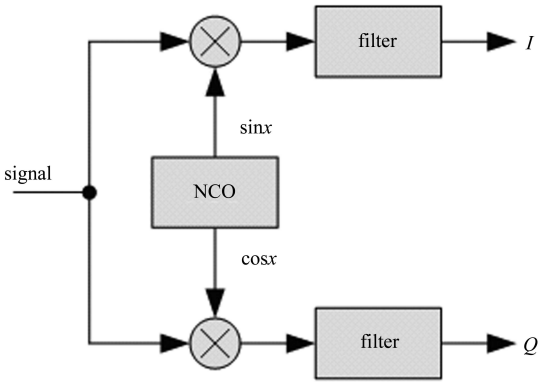

Fig. 3. The DDC architecture.

3 Calculation of the amplitude and phase

Due to the cost and the speed, many trigonometric functions are implemented using the CORDIC (Coordinate Rotation Digital Computer) algorithm in the hardware. It is a class of shift-add algorithms for rotating vectors in a plane[8, 9] (Fig. 4). The CORDIC algorithm is based on coordinate's rotation Eq. (4) from vector $[x_0, y_0]^{\mathrm{T}}$ to $[x_n, y_n]^{\mathrm{T}}$. The rotation angle θ (Eq. (6)) passes through n steps, each rotation step meets the relation Eq. (7) and the whole process of computation simplified to just shift-add.

$$\begin{bmatrix} x_n \\ y_n \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}, \tag{4}$$

$$\begin{bmatrix} x_n \\ y_n \end{bmatrix} = \frac{1}{\sqrt{1+\tan^2\theta}} \begin{bmatrix} 1 & -\tan\theta \\ \tan\theta & 1 \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}, \tag{5}$$

$$\theta=\sum_{i=0}^{n-1}\sigma_i\alpha_i,\ \sigma_i\in\{-1,1\}, \tag{6}$$

$$\tan\alpha_i=2^{-i},\quad i=0,1,2,\cdots,n-1. \tag{7}$$

I and Q can be regarded as a vector $[x,y]^{\mathrm{T}}$. Defined z parameters $\left(z_n=\sum_{i=0}^{n-1}\alpha_i\right)$ represent the angle of rotation and add these parameters to the composition of ternary vector $[x,y,z]^{\mathrm{T}}$. Suppose the initial vector is $[x_0,y_0,0]$, after several iterations the final vector $[x_n,y_n,z_n]^{\mathrm{T}}$ can be got. Controlling the direction of each iterative operational and making the y component tends to 0, we finally change the initial vector $[x_0,y_0,0]$ representation to magnitude and phase representation. Specifically the relations are as follows in Eq. (8):

$$[x_n,y_n,z_n]=\left[K\sqrt{x_0^2+y_0^2},\,0,\,\arctan\left(\frac{y_0}{x_0}\right)\right]. \tag{8}$$

Among them, $K=\prod_{i=0}^{n}\cos\left(\arctan\left(\frac{1}{2^i}\right)\right)$ is the constant determined by the number of the iteration; and the amplitude $A=x_n/K$, phase $\theta=z_n$.

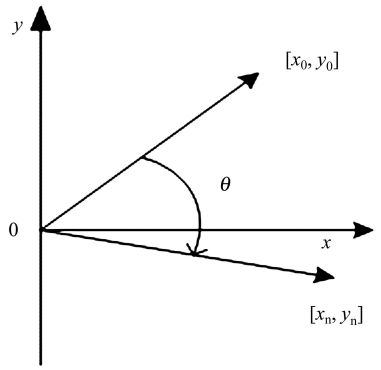

Fig. 4. The rotational diagrams.

4 Main factors affect the detection accuracy

The detection precision is affected by various factors such as jitter in the sampling clock, a defect of the algorithm itself, noises from the power system and system thermal noise, etc. The analysis of these factors will be described as follows.

a) Clock jitter

Jitter in the sampling clock will affect the system performance such as increasing the system noise and the signal's phase instability, and inducing intersymbol interference[10]. In the IF-sampling systems jitter is a big issue. The SNR (Signal to Noise Ratio) of a system can be calculated by Eq. (9)[11]. It shows that higher frequency and larger clock jitter result in lower SNR and Fig. 5 is the ENOB (Effective Number of Bits) of an ADC under corresponding clock jitter.

$$\mathrm{SNR}=-20\log(2\pi f_{\mathrm{signal}}t_{\mathrm{jitter}}) \tag{9}$$

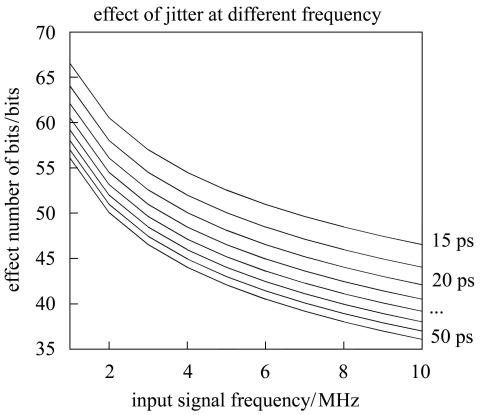

Fig. 5. Jitter and ENOB.

It is necessary to choose clock jitter on the order of femtosecond so that it is possible to achieve a higher precision (0.01°, 0.01%) detection and control in DLLRF when doing the IF sampling.

b) CORDIC algorithm error

The CORDIC algorithm has an inherent error of amplitude and phase due to the limited number of iterations and the bit cut-off in the digital fix-point system. Phase error is more evident than amplitude error. Fig. 6 (the relationship between the number of iterations and phase error (phase = −180°—180°, $n=10$—13)) shows the phase error induced by the CORDIC algorithm. A higher iteration number makes the error close to zero, the clock cycles when computing the phase.

c) ADC nonlinearity

ADC converts a continuous signal to a discrete signal and this nonlinearity will cause some harmonics in the system[12]. The quantization error of ADC and its harmonic distortion may have some relations with the ratio of f_{signal} and f_{sampling}[13, 14]. Using near-IQ sampling methods[12] we can easily distinguish the ADC harmonics in the digital domain.

d) Noise

Other noises may be produced by some factors such as switch power and other frequencies in the DLLRF system. Nearly all of the electronic systems have thermal noise and some electromagnetic interference noise; careful design can minimize these noises to make the system more reliable.

5 Experiment and result

An Altera DSP development board 2S60[15] is used to implement the algorithm, and the result will be

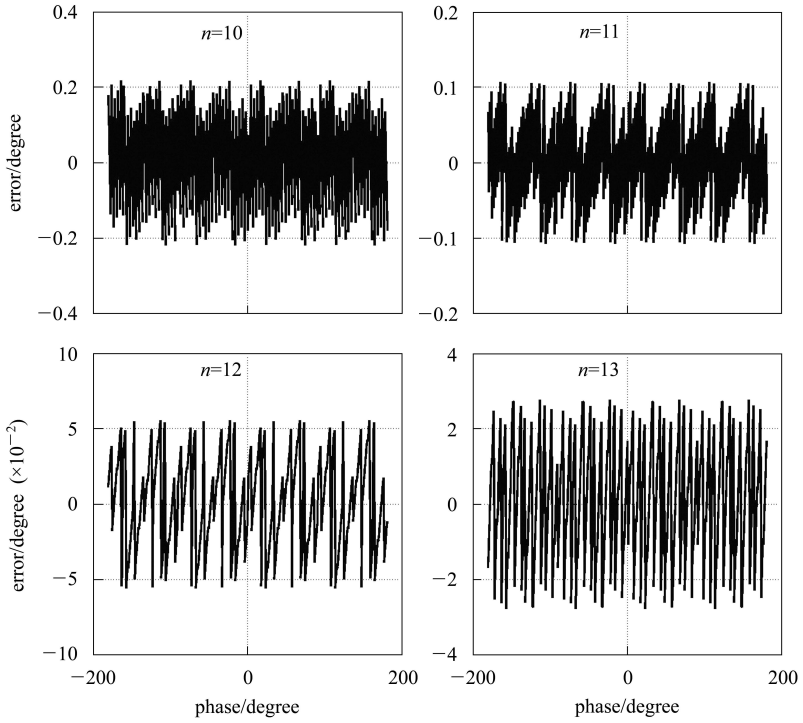

Fig. 6. The CORDIC phase error.

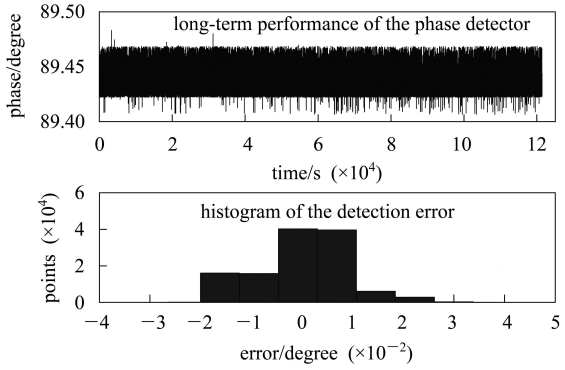

Fig. 7. Long term performance of the detector using an integer sampling method.

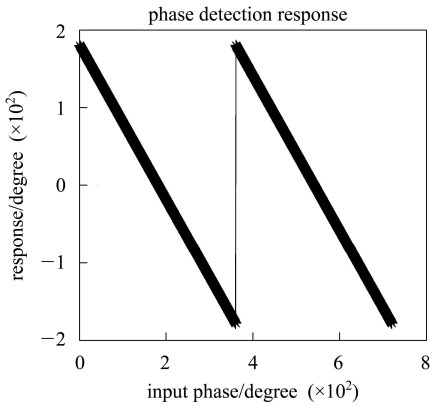

Fig. 8. The phase detection response.

observed. In this experiment, a 100 MHz sampling clock (Agilent E4428C) and a 1 MHz (Agilent 33220A) signal are chosen. The accuracy of the phase and amplitude detection is better than 0.05° and 0.02%, respectively (Fig. 7). Fig. 8 describes the phase detection response. The specification of the amplitude and phase detector implemented based on the integer number sampling method on FPGA is listed in Table 1.

Table 1. Specification.

phase resolution	$<0.05°$
phase accuracy	0.05°
amplitude resolution	<0.02%
amplitude accuracy	0.02%
detection range	−179.98° — +179.98°
amplitude dynamic range	>40 dB
bandwidth	>100 k
$\sigma_{\text{phase}}, \sigma_{\text{amplitude}}$	0.0094°, 0.008%
response time	1.3 μs

6 Conclusions

The experimental result shows that the detection error of phase resolution accuracy in real-time is less than 0.05° and the magnitude accuracy is about 0.02%. The analysis of the factors affecting the accuracy of the detection has been done. The result is helpful for future work in high precision digital low level RF control, and also for the performance improvement of any IF-sampling data acquisition and control system.

References

1 Chase B. LLRF Specs and Topics, ILC RF / Timing Workshop. FNAL, Jan. 2006
2 Simrock S. Overview of XFEL RF Specifications and Comparison to ILC Specs. ILC RF / Timing workshop, FNAL, Jan. 2006
3 LIU Yi-Lei, WANG Guang-Wei, WANG Fang. I/Q Methods Applied to Phase Detection of RF Signals. HEP & NP, 2006, **30**(8): 780—783 (in Chinese)
4 LIU Yi-Lei. I/Q Methods Applied to Amplitude and Phase Control of RF Signals. Master degree thesis (in Chinese)
5 GENG Zhe-Qiao. Design and Construction of the Phasing System for BEPC Ⅱ Linac. PhD thesis (in Chinese)
6 Grecki M. SEU-tolerant IQ Detection Algorithm for LLRF Accelerator System. Meas. Sci. Technol, 2007, **18**: 2404—2412
7 AD6636 Datasheets. http://www.analog.com
8 Volder J. The CORDIC Trigonometric Computing Technique. IRE Trans. Electronic Computing, Sept. 1959, **EC-8**: 330—334
9 Andraka R. A Survey of CORDIC Algorithms for FPGAs. FPGA '98. Feb. 22—24, 1998. 191—200
10 Brad Brannon. Aperture Uncertainty and ADC System Performance. Analog Devices, AN-501
11 KESTER W. Taking the Mystery out of the Infamous Formula, "SNR=6.02N+1,76dB" and Why You Should Care. Analog Devices, MT-001
12 Coherent Sampling vs. Window Sampling. Maxim Integrated Products. Mar. 29, 2002, AN1040
13 http://recycle.lbl.gov/∼ldoolitt/llrf/neariq.pdf and private communicate with Larry Doolittle
14 Lawrence Doolittle, MA Heng-Jie. Mark Stuart Champion. Digital Low-Level RF Control Using Non-IQ Sampling. Proc. LINAC 2006. THP004
15 Stratix II DSP Development Board Reference Manual. www.altera.com