An analogue front-end ASIC prototype designed for PMT signal readout *

Jian-Feng Liu(刘建峰)[1,2] Lei Zhao(赵雷)[1,2;1)] Li Yu(于莉)[1,2] Yu Liang(梁宇) [1,2]
Jia-Jun Qin(秦家军)[1,2] Yun-Fan Yang(杨云帆)[1,2] Wei-Hao Wu(邬维浩)[1,2]
Shu-Bin Liu(刘树彬)[1,2] Qi An(安琪) [1,2]

[1] State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China,
[2] Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

Abstract: The Water Cherenkov Detector Array (WCDA) is one of the core detectors in the Large High Altitude Air Shower Observatory (LHAASO), and it consists of 3600 photomultiplier tubes (PMTs). Both high resolution time and charge measurement are required over a large dynamic range from 1 photoelectron (P.E.) to 4000 P.E. The prototype of an analogue front-end Application Specific Integrated Circuit (ASIC) fabricated using Global Foundry 0.35 μm CMOS technology is designed to read out the PMT signal in the WCDA. This ASIC employs leading edge discrimination and an $(RC)^4$ shaping structure. Combined with the following Time-to-Digital Converter (TDC) and Analog-to-Digital Converter (ADC), both the arrival time and charge of the PMT signal can be measured. Initial test results indicate that time resolution is better than 350 ps and charge resolution is better than 10% at 1 P.E. and better than 1% with large input signals (300 P.E. to 4000 P.E.). Besides, this ASIC has a good channel-to-channel isolation of more than 84 dB and the temperature dependency of charge measurement is less than 5% in the range 0–50℃.

Keywords: analog ASIC, charge measurement, time measurement, LHAASO, WCDA

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1 Introduction

The Large High Altitude Air Shower Observatory (LHAASO) is a multipurpose complex which consists of different detectors for high energy gamma ray and cosmic ray detection [1]. A Water Cherenkov Detector Array (WCDA) will be built at LHAASO to survey gamma ray sources at energies higher than 300 GeV. The WCDA is configured with four 150 m×150 m water pools adjacent to each other. Each pool has 900 PMTs which face upward to observe the Cherenkov light produced in water by secondary particles induced by air showers [2].

The PMT signals are transmitted to the electronics via 30-m coaxial cables. The signal dynamic range of the PMT is from 1 P.E. to 4000 P.E. Within the large dynamic range, both precise time and charge measurement are required [3], as listed in Table 1.

These requirements bring quite a few challenges to the readout electronics design. Firstly, the PMT signal varies from 1 P.E to 4000 P.E. and thus a large dynamic range signal processing capability is required. Secondly, high time and charge measurement resolution within the full dynamic range is challenging, especially for 1 P.E signals, the peak current of which is as low as 60 μA (which will be further attenuated by the 30 m cable). This requires the readout electronics to have a sufficiently low noise level. Lastly, considering a 1—4000 dynamic range, the reflection of large signals could influence the measurement of subsequent small signals. Therefore, high precision impedance matching is required.

Table 1. Measurement requirements of the WCDA readout electronics in LHAASO.

parameter	requirement
channel number	3600
signal dynamic range	1 P.E.–4000 P.E.
resolution of	30%RMS@ 1 P.E.
charge measurement	3%RMS@ 4000 P.E.
RMS of time resolution	<0.5 ns RMS

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1) E-mail: zlei@ustc.edu.cn

Some large dynamic range readout ASICs for PMTs have been designed for other experiments [4-10]. However, the performance of these ASICs is not in full compliance with the requirements of WCDA in LHAASO.

In this paper, we present the design of a front-end ASIC for the time and charge measurement, to fulfill the requirements of LHAASO WCDA, with all the analogue circuits integrated within one chip. Details will be described in the following sections.

2 Circuit architecture

Figure 1 shows the architecture of the PMT readout electronics in the LHAASO WCDA. The PMT signals are sent to the readout electronics via 30 m coaxial cables, and manipulated by the ASIC. This ASIC generates two outputs: one is the output of the leading edge discrimination circuits and the other is a quasi-Gaussian signal produced by the shaping circuits, the amplitude of which corresponds to the charge information of the PMT signal. Combined with the Time-to-Digital Converter (TDC) integrated in the Field Programmable Gate Array (FPGA), time measurement can be achieved. An external Analog-to-Digital Converter (ADC) is used to digitize the quasi-Gaussian signal, and with the peak detection logic in the FPGA, the charge can be measured. Configuration of the ASIC, such as gain, test point selection and Digital-to-Analog Converter (DAC) input code, is also managed by the FPGA.

For the ASIC to cover a dynamic range up to 4000 P.E., we designed two readout channels for charge measurement: one processes the PMT anode signals to cover the range from 1 P.E. to 100 P.E., the other is used for the signal readout of the PMT tenth dynode, to cover the range from 40 to 4000 P.E. The anode signal is also fed into leading edge discriminators for time measurement in the full scale range. To achieve high precision impedance matching, an external 50 Ω resistor is used for the input signal termination of the anode channel. For the dynode channel, we use an external 20 dB π attenuation resistor network. It can achieve an equivalent input resistance of 50 Ω. Meanwhile, by adjusting the dynode signal amplitude with this resistor network and the pre-amplifier, the anode and dynode can share a similar circuit structure. With this scheme, we designed the ASIC using Global Foundry 0.35 μm CMOS technology.

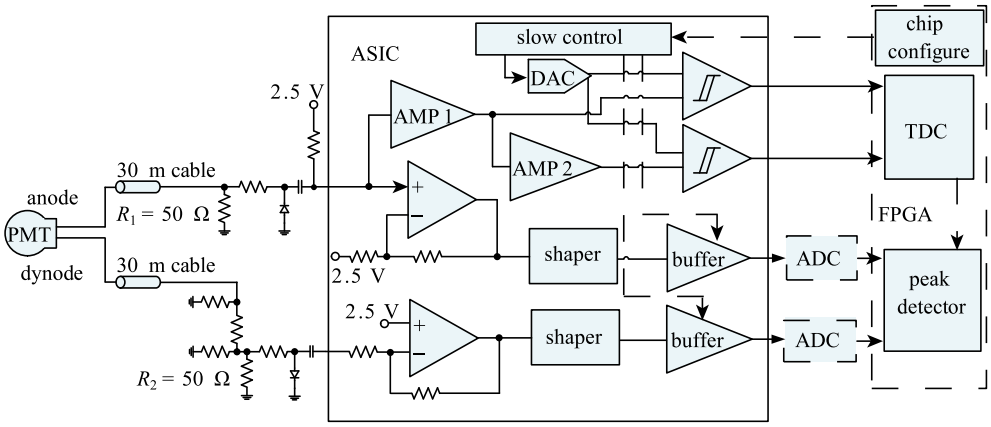

Fig. 1. Architecture of the PMT readout electronics in the LHAASO WCDA.

2.1 Basic structure of the ASIC

The detailed diagram of the anode channel is shown in Fig. 2. The anode input current signal is converted to a voltage signal on the termination resistor. Then this voltage signal is split into two paths inside the ASIC. One path is for time measurement and the other is for charge measurement.

In the time measurement part, the signal is amplified by two amplifiers, and outputs of these two amplifiers are fed into two discriminators, for which two different thresholds are selected. The thresholds are equivalent to 1/4 P.E. and 3 P.E. (user controlled in the test), respectively. The above design is aimed to avoid time resolution deterioration caused by noise or interference in the baseline of large input signals. The pre-amplifier of the time measurement part adopts a non-inverting amplification structure which features a high input impedance to avoid degrading the impedance matching precision, and it contains a differential input Operational Transconductance Amplifier (OTA), marked as A1 in Fig. 2.

For the charge measurement part, the input signal is first amplified by the OTA A2, which has a smaller bandwidth than A1. Then the amplified signal is filtered by an RC^4 shaping circuit, and driven out by a class-AB buffer which has a rail-to-rail driving capability. The shaper employs a four-order passive low-pass filter with three OTAs as the isolation stages With this structure it is easier to achieve good stability compared with active filters, e.g., a Sallen-Key filter [11].

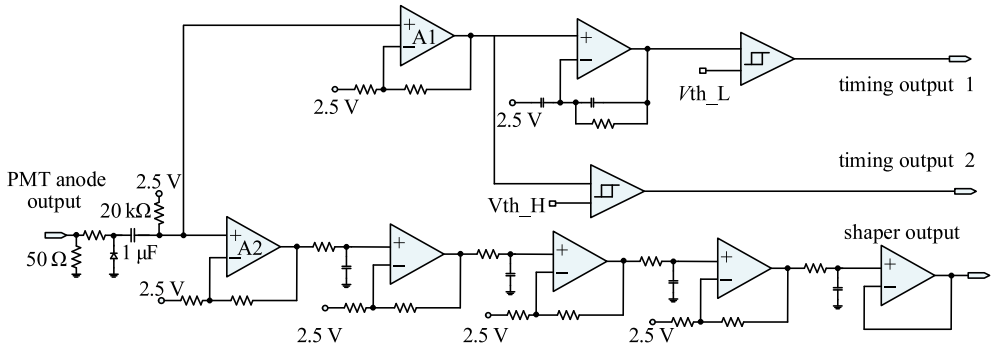

Fig. 2. Anode channel block diagram of the ASIC.

As mentioned above, the structure of the dynode channel is quite similar to the charge measurement part of the anode channel. The difference is that the pre-amplifier of the dynode channel is an inverting amplifier.

To adjust the PMT signal baseline to the input bias voltage of the ASIC, AC coupling is used at the input of the circuits, as shown in Fig. 2. Of course, if the overshoot caused by this AC coupling circuit was large, two issues would exist – decrease of the charge measurement result and input signal baseline pile-up. In our design, the 1 μF capacitor and 20 kΩ resistor constitute a first-order high pass filter with a cutoff frequency of 7.96 Hz, which is small enough. The ratio of overshoot to input signal amplitude is only 3.7×10^{-7}:1, which is negligible. As for baseline pile-up, we can estimate it. In actual experiments, most of the signals are small signals. To evaluate the baseline pile-up in a much more severe condition, we conducted simulations with a large input signal of 100 P.E. with a repetition frequency of 50 kHz. The result is that the pile-up is only 0.0371 P.E., which is good enough.

This ASIC can be configured through an SPI interface. The time and charge measurement circuits can be configured with different gains, as shown in Table 2. The DAC outputs vary over a range of 0–3.3 V with step size of 0.8 mV. It corresponds to a range of 0–20 P.E. with a step size of 0.0075 P.E. for the low threshold of time discrimination, and 0–180 P.E. with a step size of 0.06 P.E. for the high threshold. The DAC configuration code is also listed in Table 2.

Table 2. Configuration of ASIC.

parameter	range
time meas. channel gain	40, 56, 72, 104
anode charge meas.	71, 81, 90, 100,
channel gain	109, 118, 128
dynode charge meas.	23, 26, 29, 32,
channel gain	35, 38, 41
DAC for low threshold	12'h000–12'hfff (0–3.3 V)
DAC for high threshold	12'h000–12'hfff (0–3.3 V)

2.2 Pre-amplifier design

Considering the high precision and large dynamic range requirements, effort was focused on the low noise design of the pre-amplifier.

The pre-amplifier is designed based on a two-stage OTA, marked as A1 in Fig. 2. The internal structure is shown in Fig. 3. As stated in the literature [12], the input equivalent noise density is expressed in

$$\overline{v_{\rm ieq}^2}=\overline{v_{\rm R1}^2}\left(\frac{R_2}{R_2+R_1}\right)^2+\overline{v_{\rm OTA}^2}+\overline{v_{\rm R2}^2}\left(\frac{R_1}{R_2+R_1}\right)^2, \quad (1)$$

where $\overline{v_{\rm R1}^2}$, $\overline{v_{\rm R2}^2}$, and $\overline{v_{\rm OTA}^2}$ refer to the power spectral density of resistor R_1, R_2 and OTA, respectively.

In this pre-amplifier, the gain $\left(\text{i.e. } \dfrac{R_2+R_1}{R_1}\right)$ is set to 7, and Eq. (1) is approximate to

$$\overline{v_{\rm ieq}^2}=\overline{v_{\rm R1}^2}+\overline{v_{\rm OTA}^2}. \quad (2)$$

The pre-amplifier input RMS noise is the integration of its noise density over its −3 dB bandwidth. To achieve a good time resolution in time discrimination, a sufficient -3 dB bandwidth must be guaranteed. In our design, fast rise time of the PMT signal can be retained and the increase in rise time from the pre-amplifier is less than 1 ns.

So the core task is to minimize the noise density, which is contributed mainly by the OTA and R_1, as in

$$\overline{v_{\rm OTA}^2}=\frac{16}{3}kT\frac{1}{g_{\rm m1}}\left(1+\frac{g_{\rm m3}}{g_{\rm m1}}\right), \quad (3)$$

$$\overline{v_{\rm R1}^2}=4kTR_1. \quad (4)$$

In Eq. (3) $g_{\rm m1}$ and $g_{\rm m3}$ denote the transconductance of the input pair (M1, M2) and current mirror load (M3, M4) in Fig. 3.

The noise density can be reduced by increasing $g_{\rm m1}$ or decreasing the resistance of R_1, but this is accompanied with increased power consumption. Therefore, we should make a compromise between these two parameters.

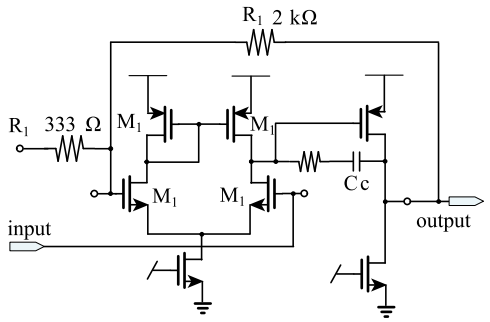

Fig. 3. Block diagram of the pre-amplifier.

For the OTA, g_{m1} and g_{m3} are optimized to be about 6 mS and 2 mS, respectively, and the consumed current is 3.6 mA. As shown in Fig. 4, the 3 dB bandwidth is 146 MHz, and the input noise is 50 μV RMS (from DC to 1 GHz), which corresponds to 1/60 P.E., beyond the application requirement. Moreover, a high Power Supply Rejection Ratio (PSRR) of 62 dB is successfully achieved, which is better than that of the single-ended input OTA often employed as low noise pre-amplifiers [4-8].

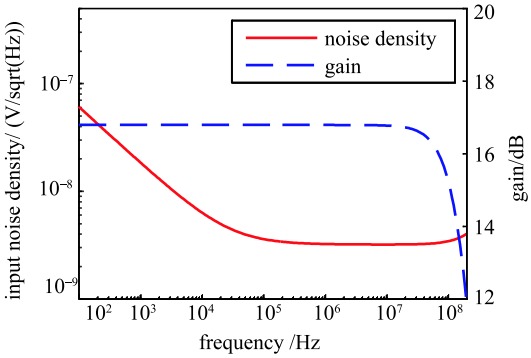

Fig. 4. (color online) Simulation results of gain and equivalent input noise density.

2.3 Low temperature drift design

Since this ASIC is applied in high altitude cosmic ray experiments without air conditioning, a low temperature drift design is necessary for this ASIC. For charge measurement, the circuits constitute an RC^n filter with a gain of 40 dB, and the output signal amplitude is expressed in

$$V_{\rm o,M}=\frac{A_v}{\tau}\frac{(n-1)^{n-1}}{(n-1)!}{\rm e}^{-(n-1)}, \tag{5}$$

where A_v and τ are the gain and time constant, respectively, of the shaping circuit, and both should be low temperature dependent.

First, A_v consists of the gains of four stages, each of which can be expressed as

$$\frac{V_{\rm out}}{V_{\rm in}}=\frac{1}{\beta}\frac{1}{1+\dfrac{1}{A_{\rm open\_loop}\beta}}, \tag{6}$$

where β is the feedback coefficient and $A_{\rm open\_loop}$ is the open loop gain of the OTA in each stage. Since β is actually the resistance ratio of two resistors, the temperature drift can be controlled to a low value when the two resistors are of the same type. As for $A_{\rm open\_loop}$, when it exceeds 60 dB, the influence on Eq. (6) caused by the fluctuation of $A_{\rm open\_loop}$ should be negligible (<0.1%).

Second, τ in Eq. (6) is actually the product of capacitance and resistance of each RC filter stage. The capacitor is almost temperature insensitive but the resistors have a relatively large temperature coefficient in Global Foundry 0.35 μm CMOS technology. To solve this problem, we designed a mixed resistor through combining two types of resistors with opposite temperature coefficients, as shown in Fig. 5.

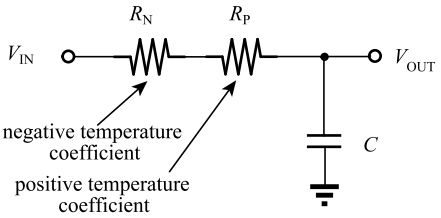

Fig. 5. Schematic of low temperature drift RC filter.

Figure 6 shows the simulation results of the resistance variation, which indicate that the temperature coefficient can be reduced to 0.3%

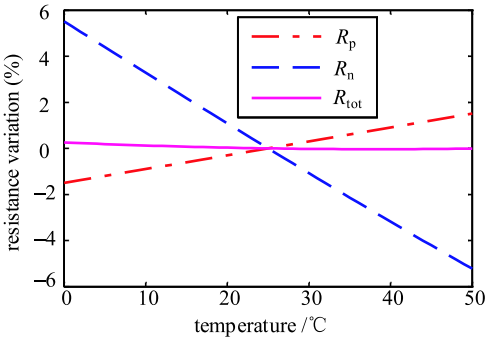

Fig. 6. (color online) Resistance variation with temperature.

As shown in Fig. 7, the simulation results indicate that the gain variation with temperature is within 0.2%. The gain variation is decided by the inherent temperature coefficient of the resistor, however, we can adjust the ratio of the two types of resistor in Fig. 5 to make $1/\tau$ have the opposite temperature coefficient and compensate the gain variation exactly. Thus the variation A_v/τ which corresponds to the output signal amplitude can be greatly reduced in the temperature range from 0 to 50 ℃as shown in Fig. 7, which is good enough for the application.

The overall charge measurement temperature drift will be presented in the next section.

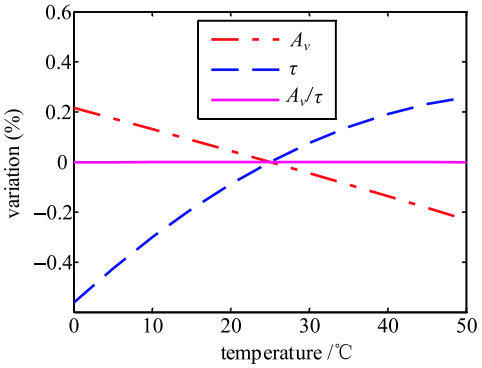

Fig. 7. (color online) Gain and time constant variation versus temperature.

2.4 Output buffer

The output buffer is responsible for driving the ASIC output signal to external ADCs for digitization. The driving capability is designed for a 50 Ω resistor and parasitic capacitance up to 10 pF. To reduce the quiescent power consumption, the output buffer employs the class-AB structure as shown in Fig. 8 [13, 14].

The input stage incorporates complementary MOS transistors to achieve a wide common mode input range. To keep the gain and bandwidth stable in this wide input range, variation of the input transconductance should be small. To achieve this, tail current compensation is incorporated, which consists of M9, M10, M11, M12, M13 and M14. We also conducted simulations to study the relationship between transconductance variation and the compensation tail current. The results indicate an optimum performance can be achieved with a specific current value.

By optimizing the parameters of the output stage MOS transistors, the ratio of dynamic and quiescent current is about 16:1. A 50 Ω resistor in parallel with a 10 pF capacitor can be driven while the quiescent power consumption is small enough. Figure 10 shows the transient simulation results of the output of this buffer with a large input amplitude, and no obvious waveform distortion is observed.

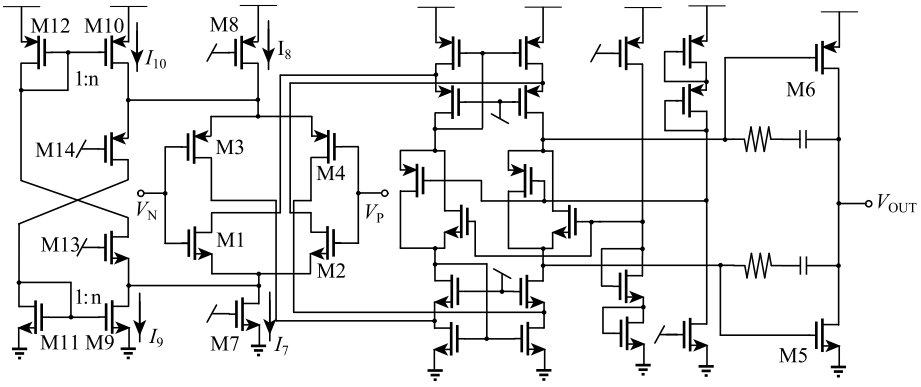

Fig. 8. Schematic of class-AB output buffer

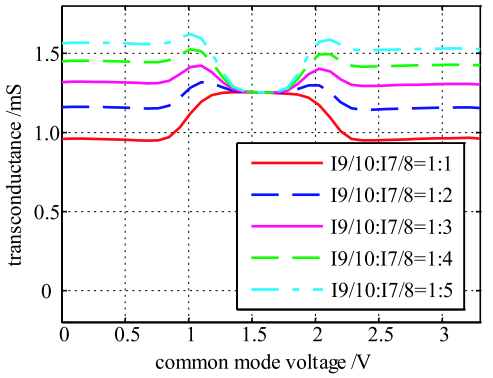

Fig. 9. (color online) Transconductance variation versus common mode voltage. Compensation tail current, I_9 and I_{10}, are the drain currents of M9 and M10 in Fig. 8.

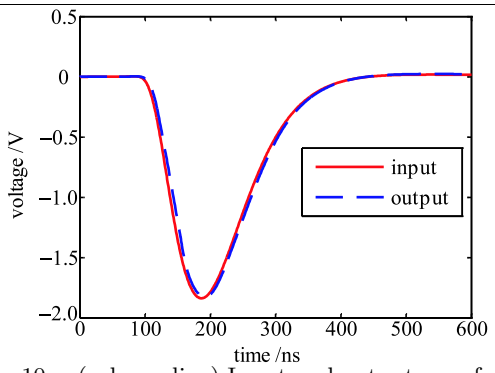

Fig. 10. (color online) Input and output waveform of class-AB buffer.

3 Simulation

A series of simulations were conducted to evaluate the overall performance of this ASIC.

Firstly, to confirm the functionality of this ASIC, we conducted transient simulations of the key nodes in the anode channel, as shown in Fig. 11. The simulation results agree well with the expected values.

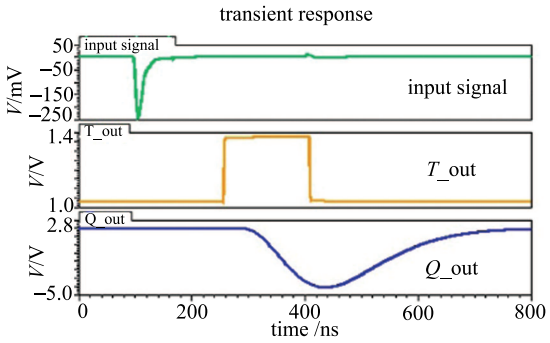

Fig. 11. (color online) Waveform simulation results of the key nodes in the anode channel.

Figure 12 shows the time resolution with different input amplitudes. In the dynamic range from 1 to 4000 P.E., the time resolution is better than 300 ps. Figure 13 shows the time walk simulation results, which are less than 20 ns in the whole range.

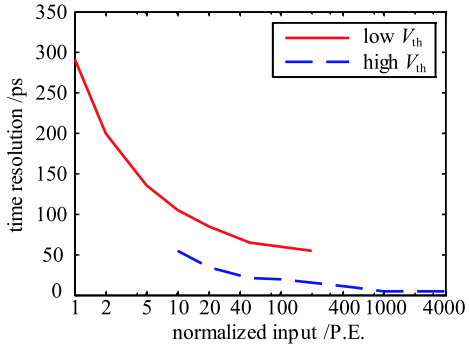

Fig. 12. (color online) Time resolution simulation results.

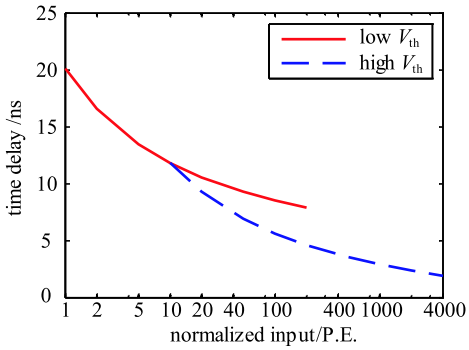

Fig. 13. (color online) Time walk simulation results.

As for charge measurement, Fig. 14 shows the ASIC output signal amplitude with different input charge, while Fig. 15 is the charge resolution simulation result, which indicates that the charge resolution is better than 10% @ 1 P.E. and 1%@ 4000 P.E.

We also conducted simulations to estimate the temperature drift performance. As shown in Fig. 16, Fig. 17 and Fig. 18, in the temperature range from 0 to 50°C, the time resolution remains better than 350 ps, while the output signal amplitude varies within ±1% and charge resolution remains better than 6%.

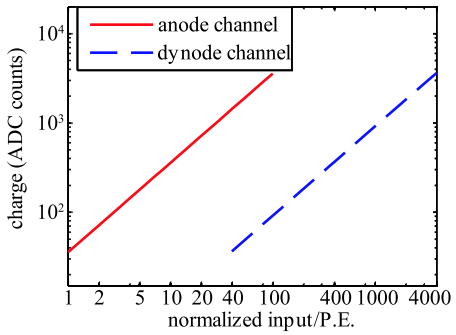

Fig. 14. (color online) Charge transfer curve simulation results.

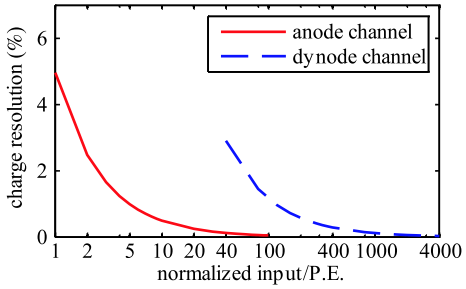

Fig. 15. (color online) Charge resolution simulation results.

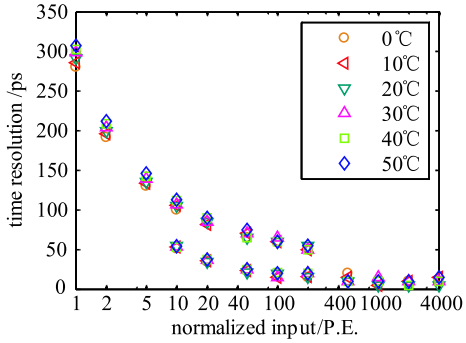

Fig. 16. (color online) Temperature dependence of time resolution.

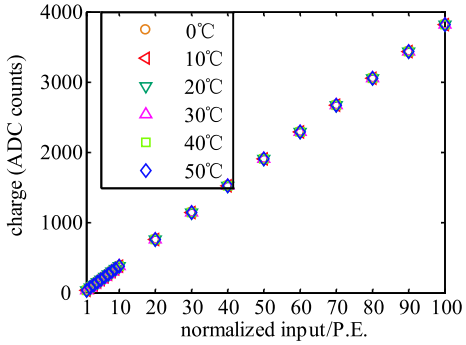

Fig. 17. (color online) Temperature dependence of charge transfer curve.

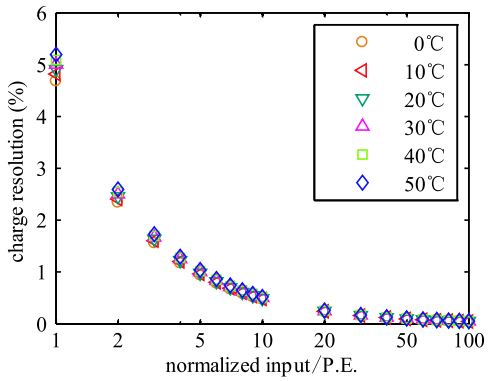

Fig. 18. (color online) Temperature dependence of charge resolution.

4 Circuit performance

After fabrication of the ASIC, we conducted a series of tests in the laboratory.

4.1 Laboratory test set-up

A dedicated test board was designed to test this ASIC. The test platform was constructed as shown in block diagram in Fig. 19. We used an arbitrary waveform signal generator (Agilent Technologies 81160A) to generate the input signal for the test, based on the waveform of the PMT (R5912) output signal acquired by the oscilloscope (Lecroy 104 MXi).

Figure 20 shows the waveform of the 1 P.E. PMT output signal, with a leading edge (10% to 90%) of 4.6 ns and a trailing edge (90% to 10%) of 16 ns. We used an attenuator (Wavetek Step Attenuator Model 5080.1) to adjust the input signal amplitude to estimate the ASIC performance in a large dynamic range. The output from the attenuator is transmitted to the ASIC evaluation board through a 30 m cable, to approximate the application situation. Then the time resolution can be tested using the oscilloscope, while the charge resolution test is conducted with a backend digitization board (with ADCs and an FPGA on it).

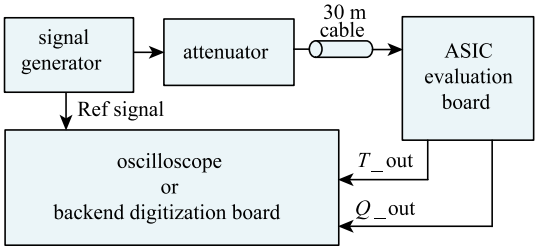

Fig. 19. Block diagram of the test platform.

Figure 21 shows a photograph of the test platform. The ASIC is marked in the middle with a yellow rectangle.

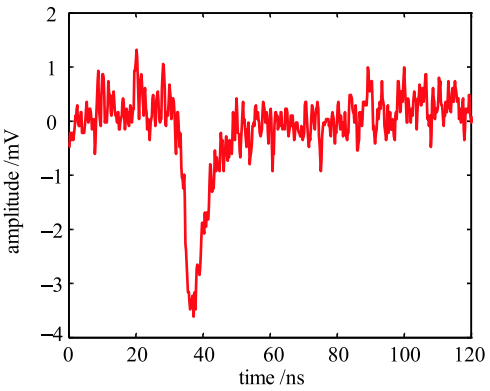

Fig. 20. Waveform of single P.E. PMT signal.

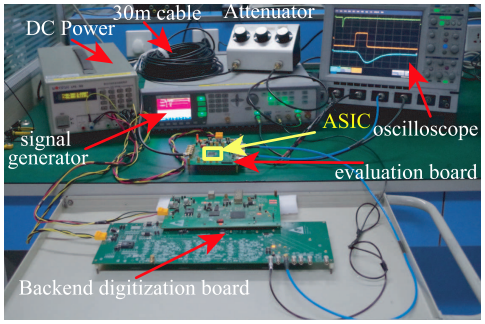

Fig. 21. (color online) Photograph of the test platform.

4.2 Basic functionality

Shown in Fig. 22 are waveform test results of the kernel nodes in the ASIC, which agree well with those in Fig. 11. The test results indicate that this prototype ASIC functions well.

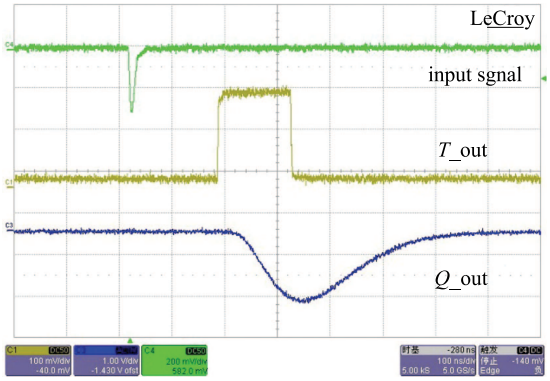

Fig. 22. (color online) Waveform test results.

4.3 Noise performance

The noise performance was investigated by measuring the output noise (RMS value) of three main blocks: the pre-amplifier in the time measurement part, the shaper of the anode channel, and the shaper of the dynode channel.

According to the test results, the intrinsic RMS noise of the oscilloscope (Tektronix DPO 7354C) is about 258.1

μV. By subtracting the above noise contribution, we can calculate the noise of the three output nodes. The worst case SNR is then further calculated (with reference to 1 P.E. for anode channel and 40 P.E. for the dynode channel). The results are listed in Table 3, also compared with the simulation results. The test and simulation results agree well, which indicates that this ASIC has good noise performance, beyond the application requirement (30% charge resolution @ 1 P.E.).

4.4 Time measurement

As shown in Fig. 19, the signal source generates two synchronous signals: one is fed into the evaluation board through an attenuator as the input signal, the other is sent to the oscilloscope as a reference signal. The delay between the "T_out" in Fig. 19 and the reference signal is measured by an oscilloscope (Lecroy 104 MXi). The statistical mean and RMS value of the delay test results correspond to time walk and resolution, respectively (the jitter between input signal and reference signal is less than 10 ps, which is negligible).

The time walk and resolution test results are shown in Fig. 23 and Fig. 24. The two curves in each figure correspond to the outputs of the discriminators with a low (1/4 P.E.) and a high (3 P.E., user controlled) thresholds, respectively. The time walk is below 15 ns and can be further calibrated according to the charge measurement results. The time resolution is better than 350 ps @ 1 P.E. and better than 100 ps with the large input signals, which concords well with the simulation results.

Table 3. The noise performance of the three main blocks.

	pre-amplifier test / simulation	anode shaper test / simulation	dynode shaper test / simulation
output voltage	18.73 mV / 18.33 mV	17.6 mV / 17.9 mV	17.84 mV / 18.4 mV
RMS noise	0.76 mV / 0.60 mV	1.12 mV / 0.84 mV	0.84 mV / 0.52 mV
SNR	24.64 / 30.55	15.71 / 21.28	21.23 / 35.38

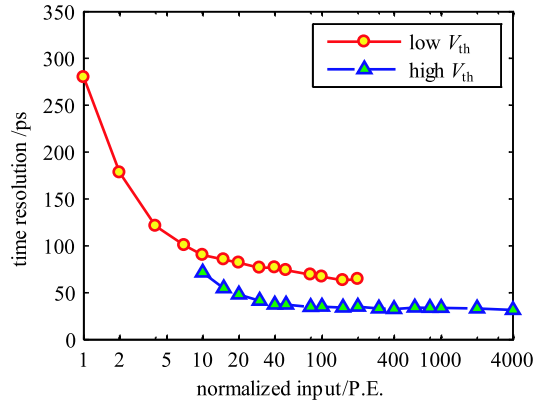

Fig. 23. (color online) Time resolution test results.

4.5 Charge measurement

As shown in Fig. 19, the shaper output "Q_out" is imported to an ADC on the backend digitization board. With the logic of the FPGA device in the same board, the peak value of the ADC output signal can be obtained, which corresponds to the charge measurement results.

Figure 25 shows the charge test results (with units of ADC count) with different input signal amplitudes. Each channel has a dynamic range of about 100 and hence two readout channels can cover the dynamic range of 4000 with a sufficient overlap. Figure 26 shows the Integral Non-Linearity (INL) test results of the charge measurement circuits. The INL are −1.4%∼0.9% and −1%∼1% for anode and dynode channel, respectively.

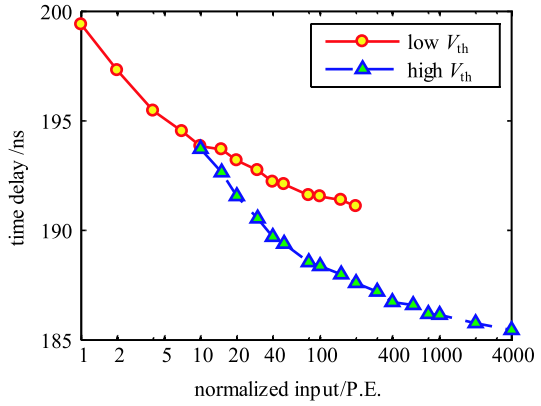

Fig. 24. (color online) Time walk test results.

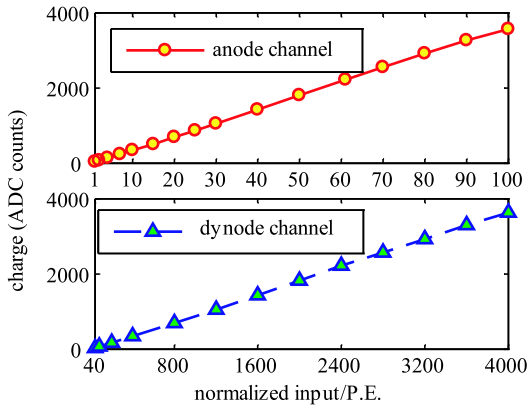

Fig. 25. (color online) Charge transfer curve test results.

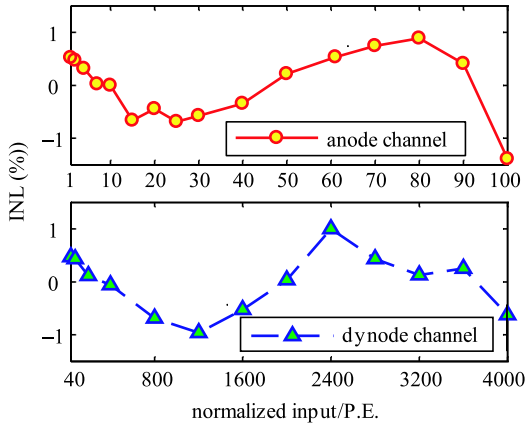

Fig. 26. (color online) INL of charge measurement test results.

Figure 27 shows the charge resolution in the full dynamic range. The overall charge resolution is better than

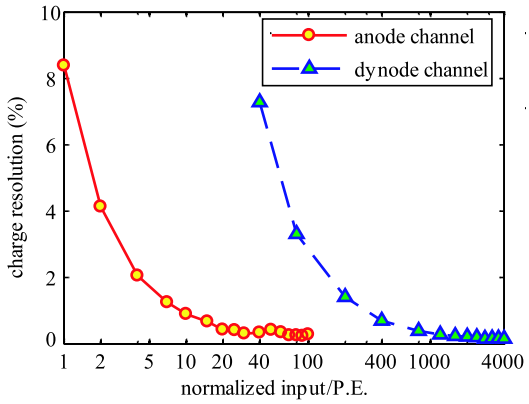

Fig. 27. (color online) Charge resolution test results.

10 % and better than 1% with input signals larger than 300 P.E., which includes the effect of the ASIC noise and the input noise of the ADC. The input noise contribution of the ADC is about 1 mV, taking the ASIC shaper noise level (shown in Table 3) into account, and hence it has a greater impact on the dynode channel charge resolution.

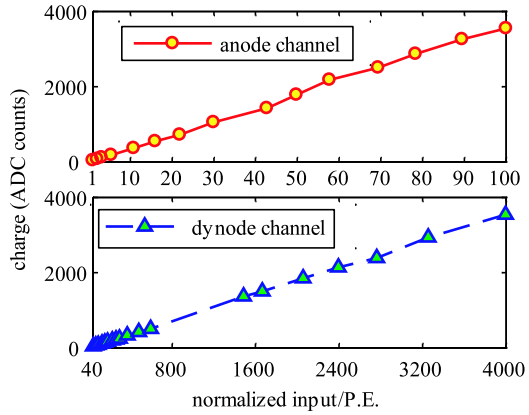

Fig. 28. (color online) Charge transfer curve test results (with real PMT).

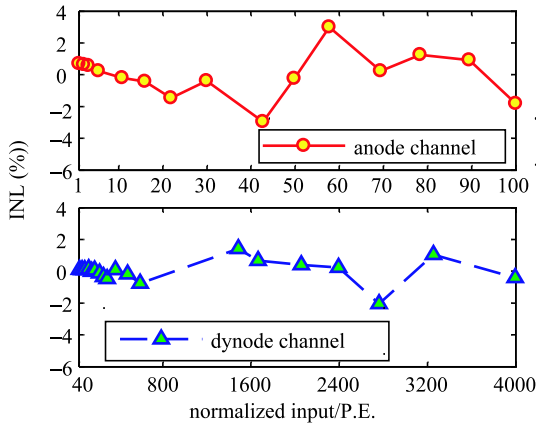

Fig. 29. (color online) INL of charge measurement test results (with real PMT).

We also conducted the charge test with a real PMT. Figure 28 and Fig. 29 show the test results with different input signal amplitudes. Fig. 29 shows the INL are −3%–3% and −2%–1.4% for anode and dynode channel, respectively.

4.6 Crosstalk

Channel isolation can be evaluated by counting error hits caused by crosstalk due to neighboring channels. No error hits (low threshold is set to 1/4 P.E.) or charge performance deterioration was observed when large signals (4000 P.E.) are imported to the neighboring channel. It indicates that this ASIC achieves a good channel-to-channel isolation performance.

4.7 Ambient temperature dependency

We also conducted temperature drift tests on this ASIC. The test temperature range was tuned from 0°C to 50°C, which covers the temperature variation of the real experiment environment.

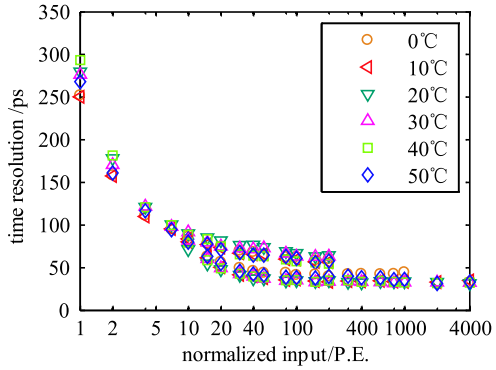

Fig. 30. (color online) Temperature dependence of time resolution.

Figure 30 shows the ambient temperature dependence of the time measurement. Within the temperature range of 0°C to 50°C, the time resolution remains better than 350 ps.

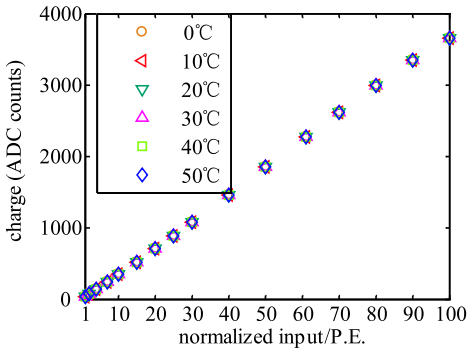

Fig. 31. (color online) Temperature dependence of charge transfer curve.

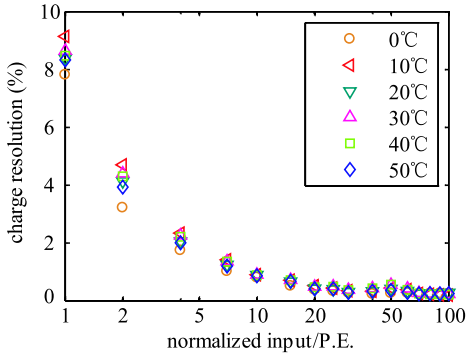

Fig. 32. (color online) Temperature dependence of charge resolution.

Figure 31 and Fig. 32 show the ambient temperature dependence of charge measurement. The charge measurement results vary within ±5% and the charge resolution remains better than 10%. The test results of temperature drift (as shown in Fig. 31) are increased by a factor of 5 compared with the simulation results (in Fig. 17). The main reason is that the temperature coefficients of the combined resistors shown in Fig. 5 will increase when the actual resistor values deviate from their nominal values.

5 Conclusions

This paper presents the design and testing of an analogue front-end ASIC prototype for PMT signal readout. This ASIC aims to fulfill precise time and charge measurement requirements for the LHAASO WCDA. The circuits are optimized to have low noise, high dynamic swing, and be temperature insensitive. A series of tests have been conducted to evaluate its performance. Test results indicate that the time resolution is better than 350 ps in the full dynamic range and charge resolution is better than 10% @ 1 P.E. and better than 1% for input signals larger than 300 P.E. Meanwhile, this ASIC has been proven to have high channel-to-channel isolation and weak ambient temperature dependency.

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