Application of stratified implantation for silicon micro-strip detectors*

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Abstract: In the fabrication of a 48 mm×48 mm silicon micro-strip nuclear radiation detector with 96 strips on each side, a perfect P-N junction cannot be formed consistently by the one-step implantation process, and thus over 50% of strips produced do not meet application requirements. However, the method of stratified implantation not only avoids the P region between the surface of wafers and the P^+ region, but also overcomes the shadow effect. With the help of the stratified implantation process, a perfect functional P-N junction can be formed, and over 95% of strips meet application requirements.

Key words: nuclear radiation detectors, stratified implantation, P-N junction, reverse body resistance

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1 Introduction

With the development of the ultra large scale integrated circuit, devices with smaller crucial sizes and larger chip areas are needed, and the traditional thermal diffusion process is commonly replaced by the implantation technique. Ion implantation has the unique advantage that the number and depth of the implanted ions in the device can be precisely controlled, so the device can be easily duplicated. Compared to the high-temperature diffusion process, ion implantation can be done at room temperature, which also reduces the value of the thermal budget. Ion implantation is a physical process, no chemical reaction occurs. The implantation process has been widely adopted, with one important purpose being to implant semiconductor ions. It has become a standard process for 0.25 μm feature size and ultra large chips in modern semiconductor processes [1–7].

In the fabrication of a 48 mm×48 mm silicon micro-strip nuclear radiation detector with 96 strips on each side in our laboratory, a process of one-step B^+ implantation was initially adopted, but unfortunately, more than 50% of the strips could not form a steady P-N junction. Based on the simulation result from Silvaco code, the one-step B^+ implantation process was replaced by a stratified implantation process in the fabrication of the silicon micro-strip detector.

2 Experimental method

The silicon micro-strip detector was fabricated using MEMS (Micro Electro Mechanical Systems) techniques. 4-inch wafers were lightly doped with 10^{12} atoms/cm^3 N-type dopant to achieve a good surface resistivity higher than 5000 Ω·cm. The wafers were then cleaned with a routine RCA ("standard clean") cleaning procedure. An oxidation film with a thickness of 6000 Å was then grown on the wafers in an oxidation furnace at 1030 ℃ for 4 hours. After that, the micro-strip patterns were transferred to the wafers by a lithography machine. The wafers were further treated with a boron implantation at the top surface and a phosphorus implantation at the back surface by a medium-energy ion implanter, and a silicon strip detector sample was thus achieved.

The detector's sensitive area is 48 mm×48 mm and the thickness is 300 μm. Both sides of the surface were divided into 96 equal strips with an element pitch of 500 μm by oxide separation of 50 μm. Each strip is a P-N junction. More detailed information about the detector can be found in Ref. [8].

According to the application requirement and the process parameters, a large amount of B^+ ions at 40 keV and 1.5×10^{14} ions/cm^2 have been implanted into the wafers. It is found that more than 50% of the micro strips cannot form a functional P-N junction. Their reverse

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body resistances are normally lower than 20 MΩ·cm, and thus result in high leakage current and bad energy resolution for heavy ion particles, which obviously does not meet our experimental requirement. Based on the suggestion of simulation results (below), the process of stratified implantation was then applied with the following procedures. B^+ ions were firstly implanted into the wafer at 40 keV, 2×10^{14} ions/cm^2, and then sequentially implanted at 20 keV, 2×10^{14} ions/cm^2 into the same wafers. Preliminary test results show that over 95% of the silicon micro-strips in this batch have a perfect P-N junction with reverse body resistance larger than 500 MΩ·cm. The energy resolution for 5.156 MeV α particles of ^{239}Pu source is about 0.8% or even less, the test results are shown in Fig. 1. This could meet the application requirements for nuclear experiments.

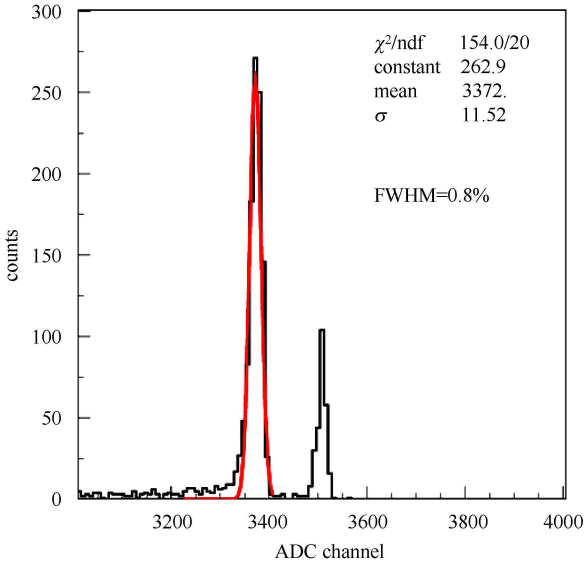

Fig. 1. (colour online). Test results of energy resolution for 5.156 MeV α particles of a ^{239}Pu source.

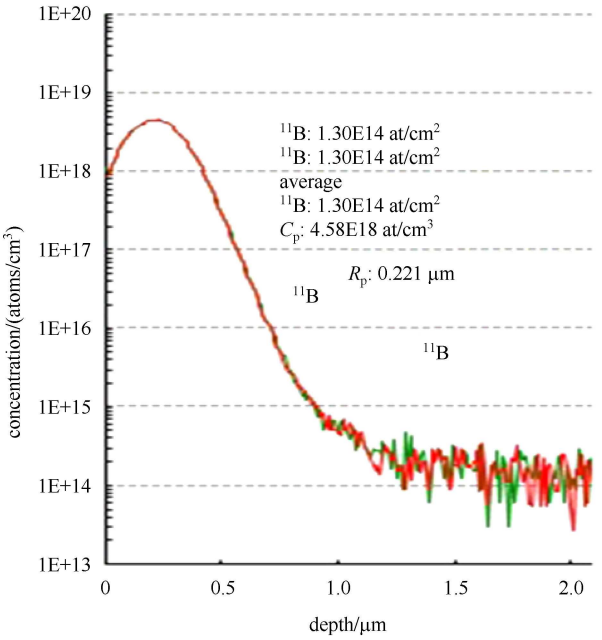

Fig. 2. (colour online). SIMS test results for the one-step implanted chips.

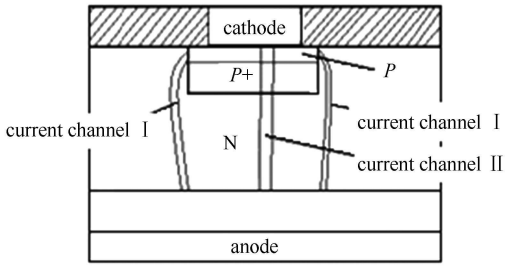

Fig. 3. Schematic of a P-P$^+$-N structure with two current channels. Most of the reverse current flows along current channel Ⅰ.

3 Results and discussion

To interpret this phenomenon, a SIMS (secondary ion mass spectrometry) test was done for the malfunctioning chips fabricated with the one-step implantation process. The implanted atoms were activated by annealing at 1030 ℃ for 30 min, allowing them to diffuse further. The test results are shown in Fig. 2. The red and green lines are the SIMS test results with two different points.

The test result tells us that the peak value (C_p) of B^+ concentration appears at 0.221 μm away from the wafer top surface with a concentration of 4.58×10^{18} atoms/cm^3. The top surface B^+ concentration is only 8×10^{17} atoms/cm^3, 1/6 of the peak value. The structure of the detectors is therefore definitely different from the designed devices shown in Fig. 1, being more like a P-P$^+$-N structure as shown in Fig. 3.

According to Fig. 3, when the reverse body resistance of the chips is tested as an indicator, most of the leakage current from anode to cathode will flow through channel Ⅰ. Eq. (1) shows the reverse saturation current density for a P-N junction [9],

$$\frac{qD_p p_{n0}}{L_p}+\frac{qD_n n_{p0}}{L_n}=J_s, \tag{1}$$

where q is the unit electric charge; D_p is the diffusion coefficient for holes; p_{n0} is p_n at thermal equilibrium (p_n is the hole concentration in N-type semiconductor (minority carriers)); L_p is the diffusion length of holes; D_n is the diffusion coefficient for electrons; n_{p0} is n_p at thermal equilibrium (n_p is the electron concentration in P-type semiconductor (minority carriers)); L_n is the diffusion length of electrons; and J_s is the saturation-current density.

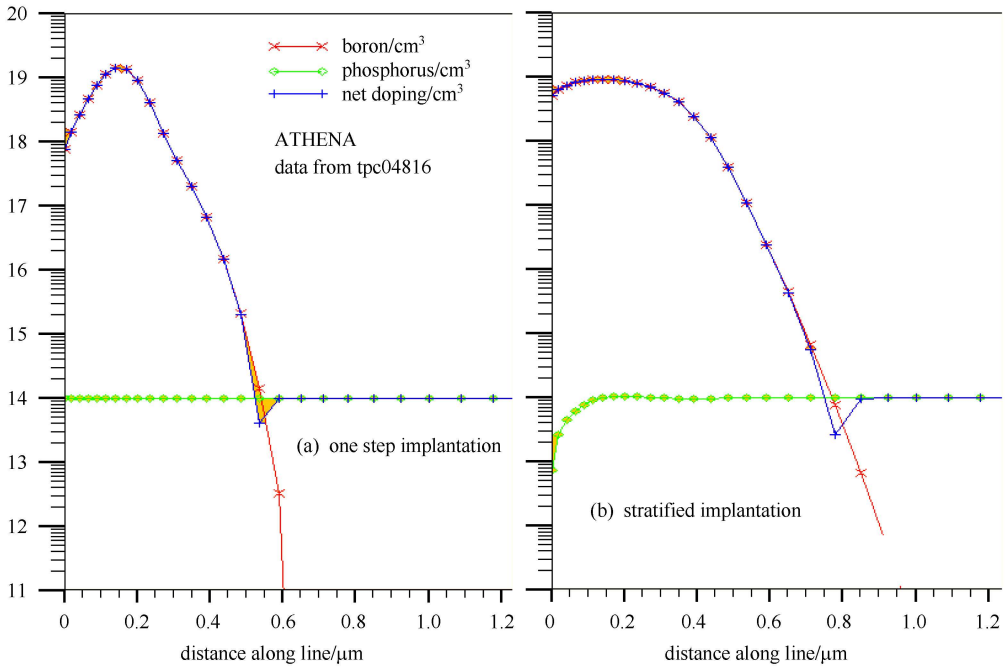

Fig. 4. (colour online) Simulated scheme of a P^{++}-P^{+}-N structure fabricated with stratified B^{+} implantation.

Channel Ⅰ is from a P-N junction and channel Ⅱ is from a P^{+}-N junction. According to Eq. (1), the first part of Formula is same for the P-P^{+}-N and P^{+}-N, while the second part is obviously different. J_s through channel Ⅰ is much higher than J_s through channel Ⅱ, which implies that most of the leakage current flows through channel Ⅰ. This device works more like a P-N junction than the desired P^{+}-N junction.

The samples fabricated with the stratified B^{+} implantation technique (first 40 keV, 2×10^{14} ions/cm^2, then 20 keV, 2×10^{14} ions/m^2) were simulated with Silvaco code. The simulation result is shown in Fig. 4.

The structure of this device is a type of P^{++}-P^{+}-N, as shown in the right part of Fig. 4, which is a standard P-N junction, so most of the leakage current from anode to cathode flows through the central channel, and thus the reverse body resistance of the device will be much higher than that of the device fabricated by one-step implantation. This could improve the electric properties of the device.

The avoidance of the shadow effect may make another contribution to the improvement of the chip's performance. As is well known, the shadow effect is inevitable in one-step implantation. In the actual operation of the ion implanter, there is always a 7° angle between the wafers and the ion beam to avoid the ion-channel effect, but this 7° angle can lead to the shadow effect. For example, if the mask is 0.5 μm thick, the 7° angle will lead to a 61 nm shadow on the chip surface, which means that this area remains in the N type without B^{+} implantation.

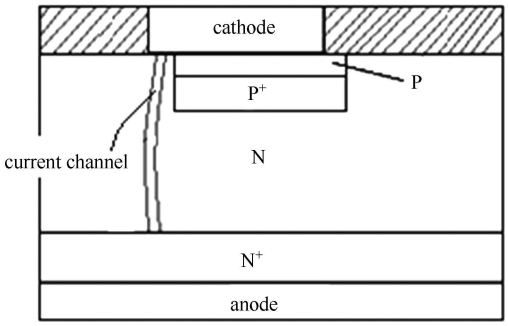

Fig. 5. Schematic of a N^{+}-N structure fabricated by the shadow effect, with all reverse current following the current channel.

The chip will work as N-N^{+} device in this region, besides the previously mentioned P-P^{+}-N device. The leakage current from the anode to cathode follows the channels shown in Fig. 5.

The devices fabricated under stratified B^{+} implantation not only realize the structure of a standard P-N junction, P^{++}-P^{+}-N, but can also overcome the problem of the shadow effect. Since the wafers reloaded on the ion implanter mostly have their orientation changed compared to the last implantation, the current implantation could cover the shadow region left by the last implantation, consequently overcoming the shadow effect. The final effect of multi-step implantations is shown in Fig. 6. No P region or N region is left on or near the surface. The chips with P^{++}-P^{+}-N-N^{+} works as a perfect P-N junction.

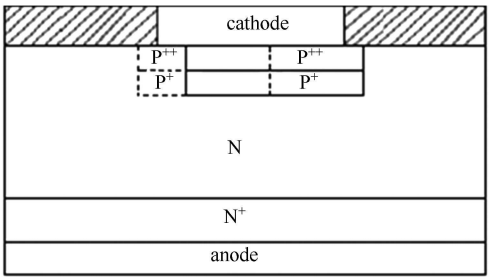

Fig. 6. Schematic diagram of the chips fabricated with stratified implantations.

4 Conclusions

One-step implantation for nuclear detectors cannot fabricate a perfect P-N junction. More than 50% of the strips produced in this experiment had bad reverse body resistances and could not meet experimental requirements. This is due to the structure of this kind of device, where a P region occurs between the surface of the wafers and the P^+ region. Another reason is the existence of a shadow region because of the shadow effect. The process of stratified implantation can effectively avoid the P region between the surface of the wafer and the P^+ region, and can also overcome the shadow effect because the second implantation can implant the ions into the shadow region left by the first implantation. Finally almost all the reverse current follows the central P-N junction channel and the reverse body resistance significantly increases. For micro-strip detectors fabricated by the stratified B^+ implantation process, about 95%, can meet most of the experimental requirements. The stratified B^+ implantation method will become an essential process in the future fabrication of silicon micro-strip detectors.

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